BME2322 – Logic Design

The Instructors:

Dr. Görkem SERBES (C317)

gserbes@yildiz.edu.tr

https://avesis.yildiz.edu.tr/gserbes/

Lab Assistants:

Nihat AKKAN

nakkan@yildiz.edu.tr

https://avesis.yildiz.edu.tr/nakkan

LECTURE 2

Concrete Encoding of Information

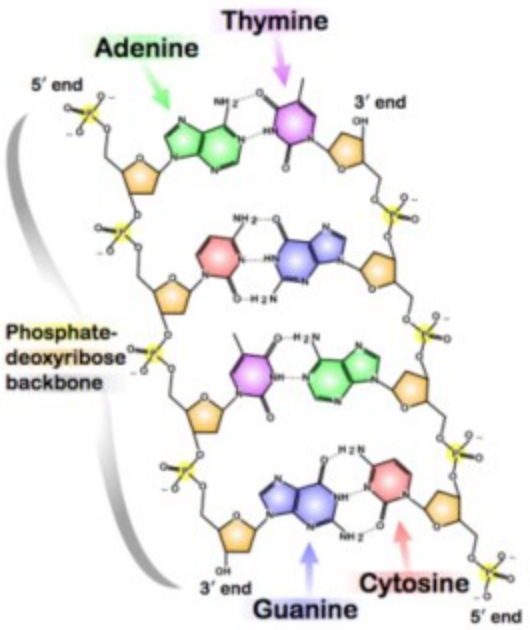
To this point we've discussed encoding information using bits. But where do bits come from?

If we're going to design a machine that manipulates information, how should that information be physically encoded?

Rosetta Stone

Captmondo (CC BY-SA 3.0)

DNA



Madeleine Price Ball (CC BY-SA 3.0)

What makes a good bit?

- small, inexpensive (we want a lot of them)
- stable (reliable, repeatable)
- ease and speed of manipulation
  (access, transform, combine, transmit, store)

We may Use Electrical Phenomenon

Consider using phenomenon associated with charged particles:

voltages	phase
currents	frequency

In this course we'll use voltages to encode information. But the best choice depends on the intended application…

Voltage pros:

- easy generation, detection
- lots of engineering knowledge
- potentially ~~low~~ zero power in steady state

Voltage cons:

- easily affected by environment
- DC connectivity required?
- R & C effects slow things down

Representing Information with Voltage

Representation of each (x,y) point on a B&W image:

0 volts:	BLACK
1 volt:	WHITE
0.37 volts:	37% Gray

John Phelan (CC BY 3.0)

How much information at each point?

Suppose we can reliably distinguish voltages that differ by $1/2^N$ volts. Then we can represent N bits of information by voltages in the range 0V to 1V. What are realistic values for N?

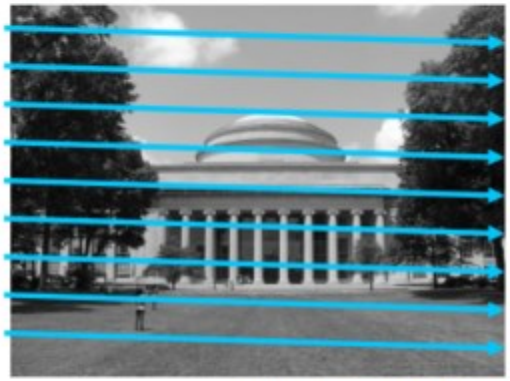
We use analog signals

Using Analog Voltages to Encode a Picture

Representation of a picture:

Scan points in some prescribed raster order…

Generate voltage waveform:



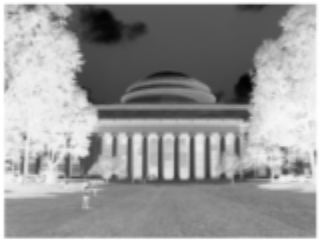
John Phelan (CC BY 3.0)

Information Processing = Analog Computation

Information Processing = Computation

v → Copy → v

v → Inv → 1-v



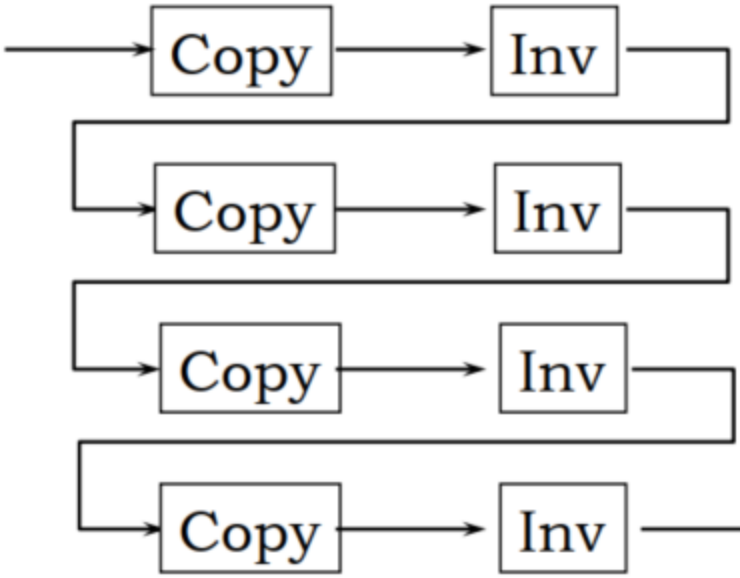
Why have processing blocks?

- Pre-packaged functionality: rely on behavior without having to be an analog engineer
- Predictable composition of functions
  → Tinker-toy assembly
- Guaranteed behavior:
  if components work, system will work!

Wow, rules simple enough for a programmer to follow!

Let's Build an Analog System!

input

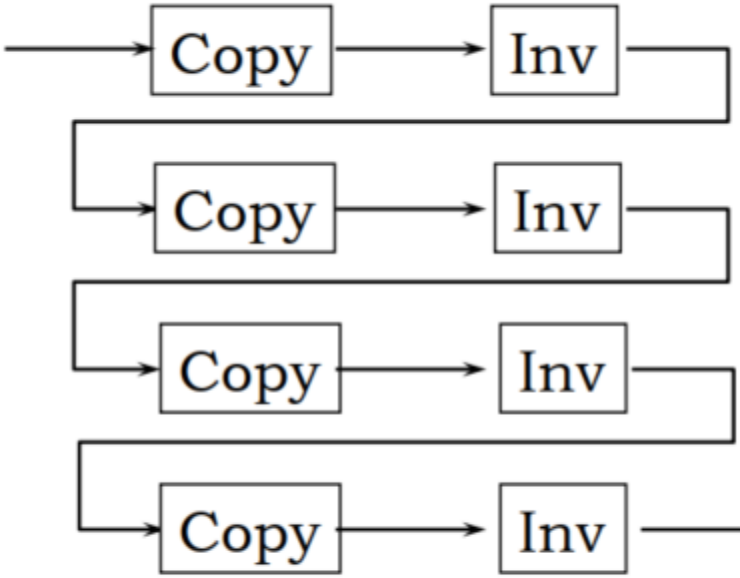


Expected

output

Let's Build an Analog System! (cont.)

input



(Reality)

output

Why Did Our System Fail?

Why doesn't theory match reality?

1. COPY block doesn't work right
2. INV block doesn't work right
3. Theory is imperfect
4. Reality is imperfect
5. Our system architecture stinks

Why Did Our System Fail?

Why doesn't theory match reality?

1. COPY block doesn't work right
2. INV block doesn't work right
3. Theory is imperfect
4. Reality is imperfect
5. Our system architecture stinks

ANSWER: all of the above!

Noise and inaccuracy are inevitable; we can't reliably reproduce infinite information – we must design our system to tolerate some amount of error if it is to process information reliably.

Example 1

Consider an analog image processing system built entirely from COPY blocks, which when given V volts on their input are designed to produce V volts on their output. Armo, an inexpensive brand of COPY blocks, comes close to meeting the specification, but produces an output with up to a 1% error. So for a V volt input, an Armo COPY block will produce an output voltage in the range $0.99 \cdot V$ to $1.01 \cdot V$.

If an Armo COPY block has an input of 0.5 volts, what are the smallest and largest voltages we might measure on its output? Please give a numeric answer to the nearest .001 volt.

Smallest output voltage (volts):

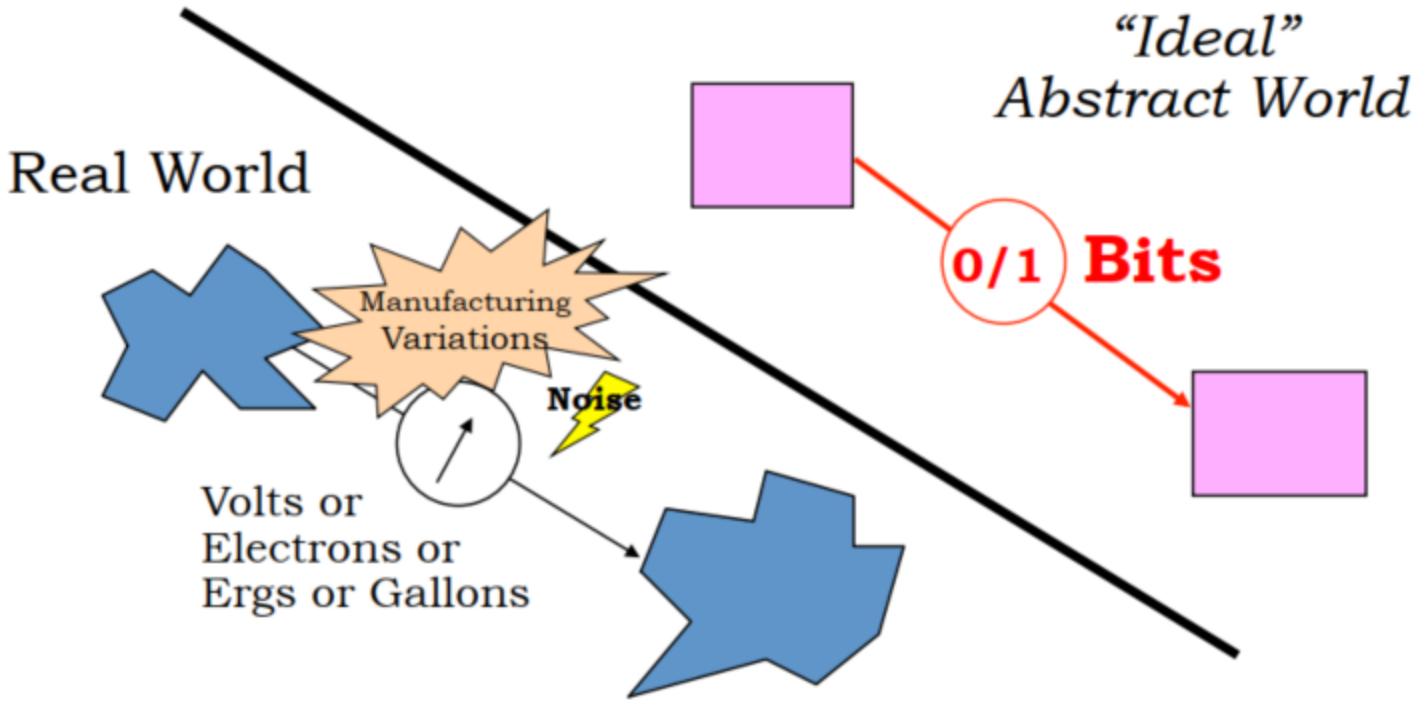
Largest output voltage (volts):

Now consider a system that uses 50 Armo COPY blocks connected in series, i.e., the output of one block is connected to the input of the next block. If a signal of 0.5 volts is input to the first block in the series, what is the range of voltages we might measure on the output of the fiftieth block? Please give a numeric answer to the nearest .001 volt. Hint: the answer is *not* simply an increase or decrease of $0.01 \cdot 0.5 \cdot 50$ volts.

Smallest output voltage (volts):

Largest output voltage (volts):

The Digital Abstraction

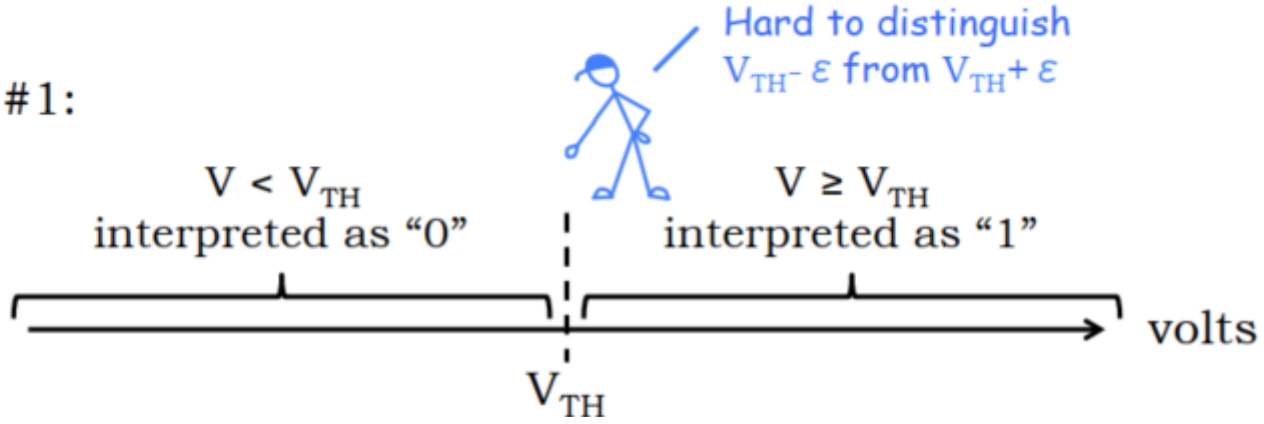


Keep in mind that the world is not digital, we would simply like to engineer it to behave that way. Furthermore, we must use real physical phenomena to implement digital designs!

Using Voltages 'Digitally'

- Key idea: encode only one bit of information: 2 values "0", "1"
- Use the same uniform representation convention for *every* component and wire in our digital system

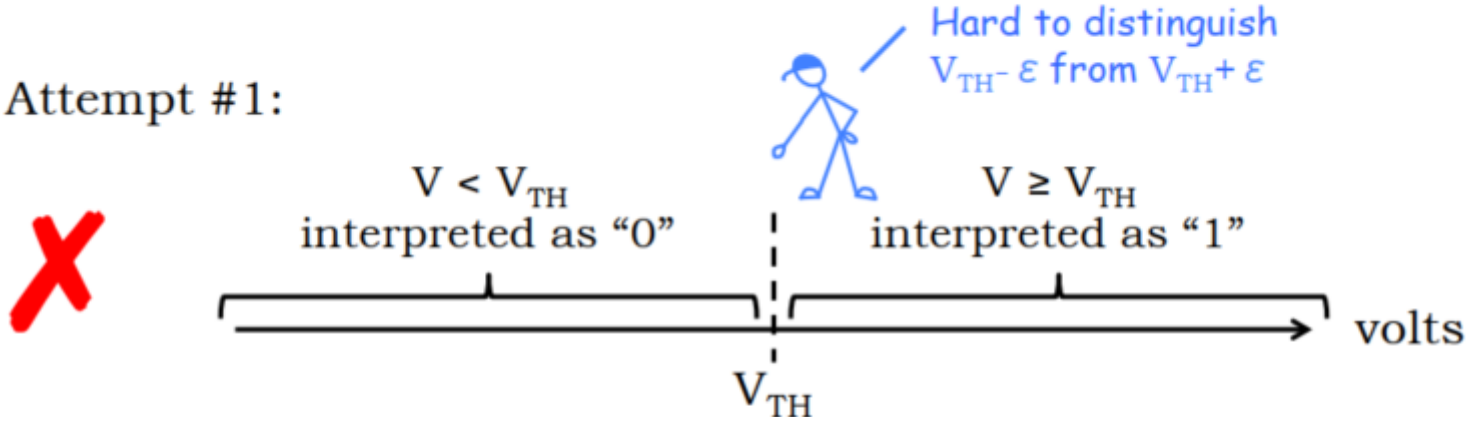
Attempt #1:



Using Voltages 'Digitally'

- Key idea: encode only one bit of information: 2 values "0", "1"
- Use the same uniform representation convention for *every* component and wire in our digital system

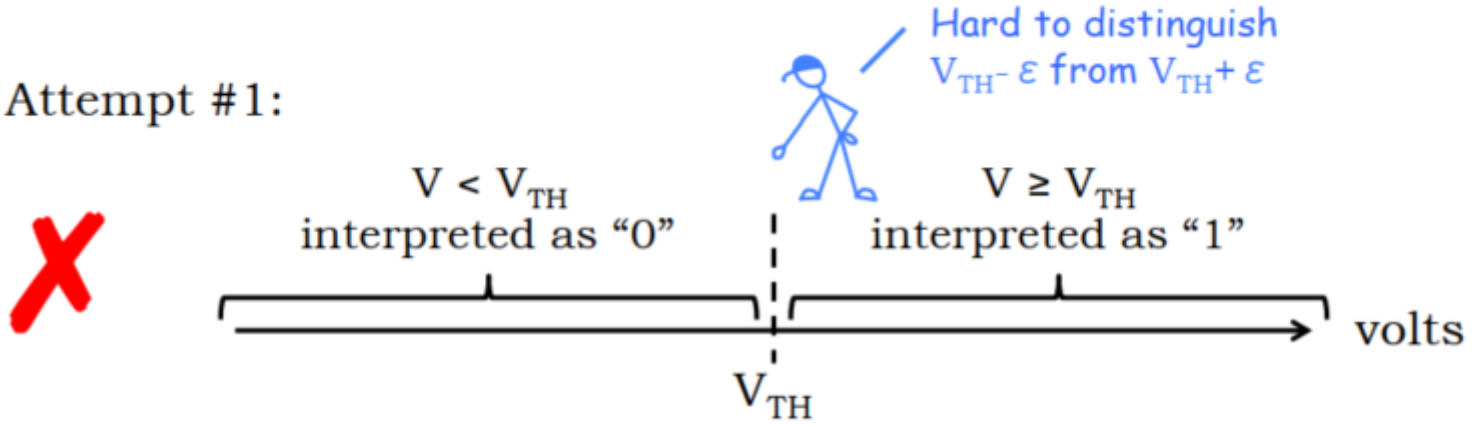
Attempt #1:



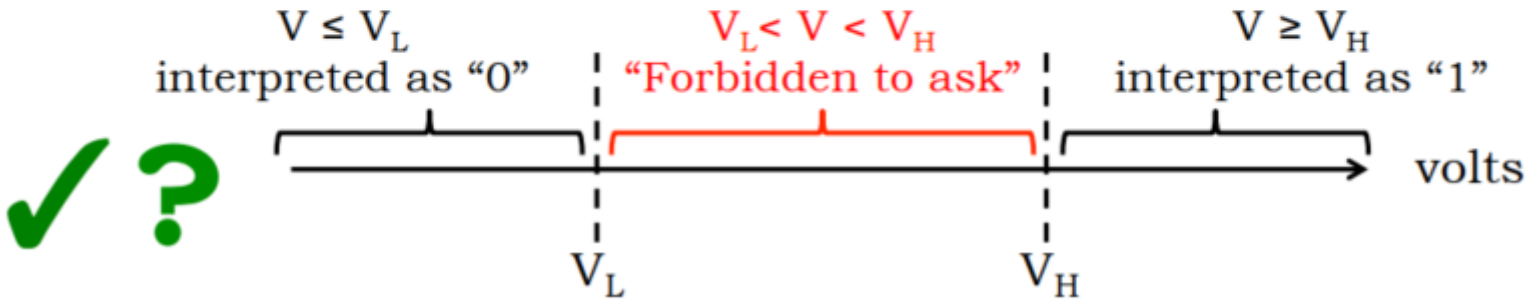
Using Voltages 'Digitally'

- Key idea: encode only one bit of information: 2 values "0", "1"
- Use the same uniform representation convention for *every* component and wire in our digital system

Attempt #1:



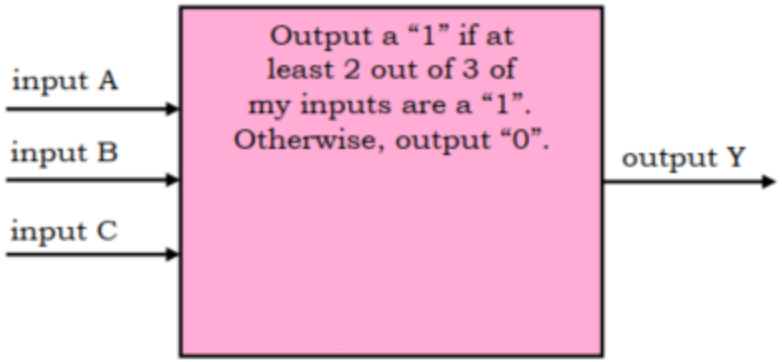
Attempt #2:



A Digital Processing Element

A combinational device is a circuit element that has

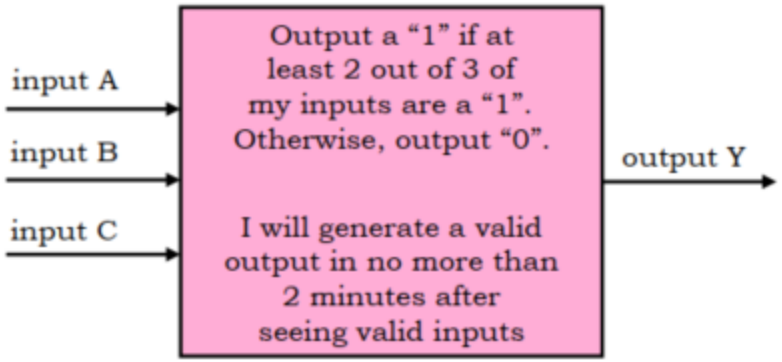
- one or more digital *inputs*
- one or more digital *outputs*
- a *functional specification* that details the value of each output for every possible combination of valid input values



A Digital Processing Element

A combinational device is a circuit element that has

- one or more digital *inputs*
- one or more digital *outputs*
- a *functional specification* that details the value of each output for every possible combination of valid input values
- a *timing specification* consisting (at minimum) of an upper bound t_{PD} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values

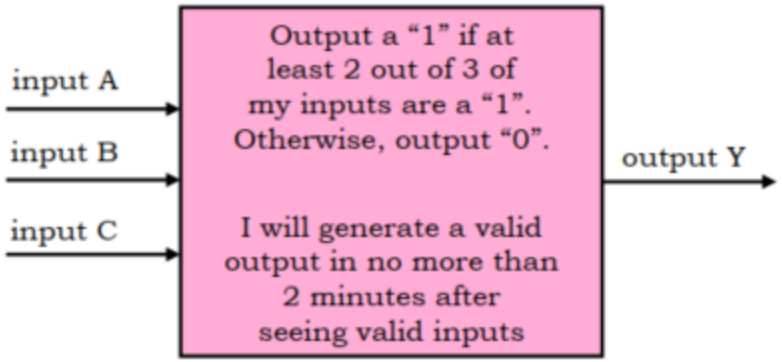


A Digital Processing Element

A combinational device is a circuit element that has

Static discipline

- one or more digital *inputs*
- one or more digital *outputs*
- a *functional specification* that details the value of each output for every possible combination of valid input values
- a *timing specification* consisting (at minimum) of an upper bound t_{PD} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values



A Combinational Digital System

A set of interconnected elements is a combinational device if

- each circuit element is combinational
- every input is connected to exactly one output or to some vast supply of constant 0's and 1's
- the circuit contains no directed cycles

A Combinational Digital System

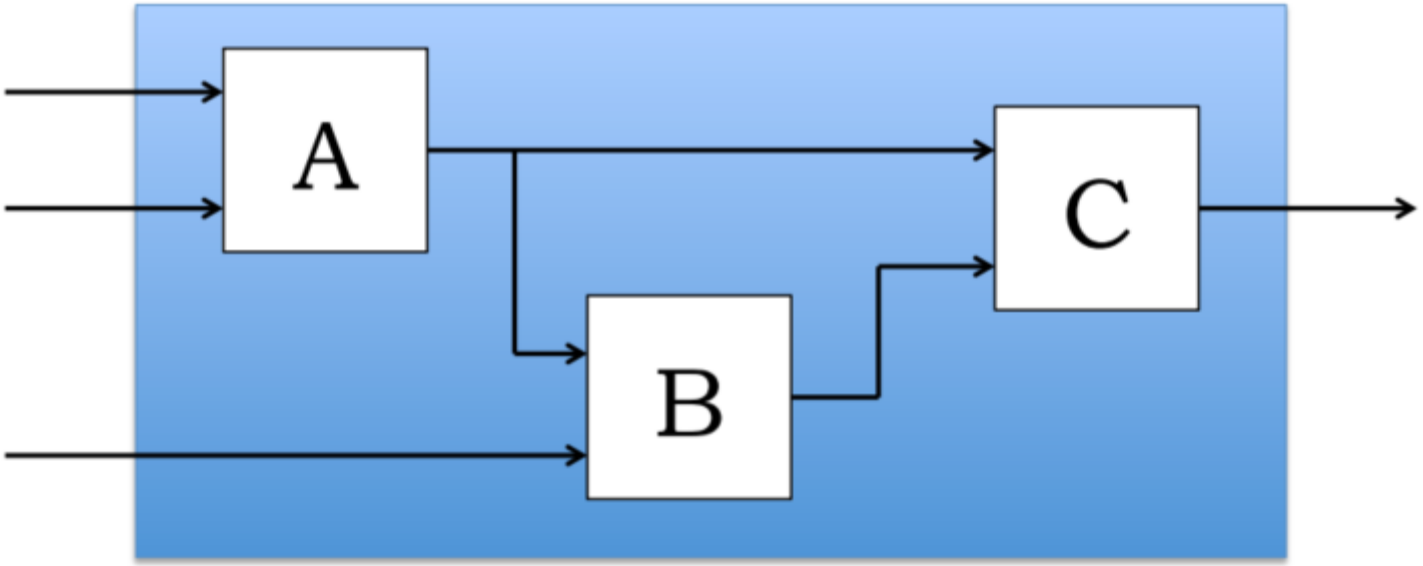
A set of interconnected elements is a combinational device if

- each circuit element is combinational
- every input is connected to exactly one output or to some vast supply of constant 0's and 1's
- the circuit contains no directed cycles

Why is this true?

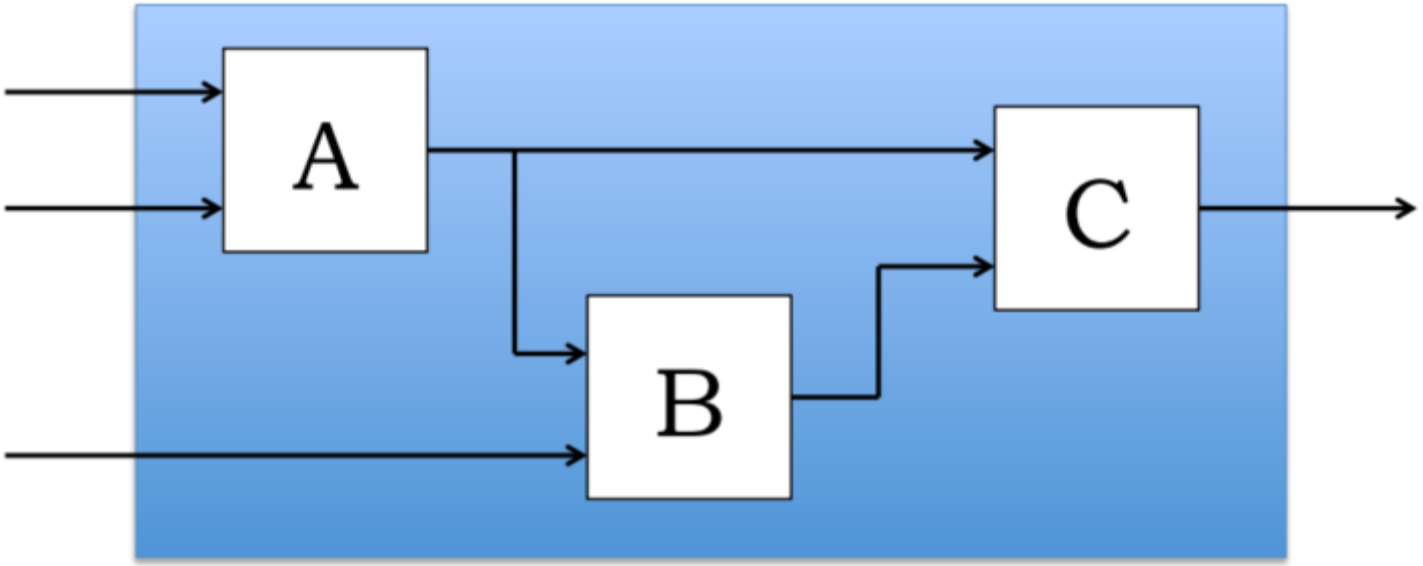
Is This a Combinational Device?

A, B and C are combinational devices. Is the following circuit a combinational device?



Is This a Combinational Device?

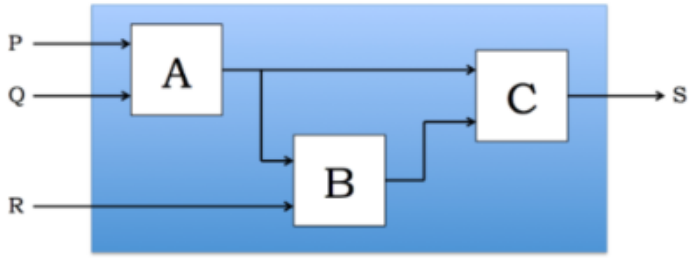
A, B and C are combinational devices. Is the following circuit a combinational device?



- Does it have digital inputs?
- Does it have digital outputs?
- Can you derive a functional description?
- Can you derive a t_{PD}?

Example 2

Let's roll up our sleeves and try to build the functional and timing specifications for a system of combinational devices using the specifications of the component devices. We'll use the system diagram from the previous video:



And here are the specifications for the A, B, and C components:

x	y	A(x,y)
0	0	0
0	1	0
1	0	0
1	1	1

x	y	B(x,y)
0	0	0
0	1	1
1	0	1
1	1	1

x	y	C(x,y)
0	0	0
0	1	1
1	0	1
1	1	0

$t_{PD,A} = 3\text{ns}$ $t_{PD,B} = 2\text{ns}$ $t_{PD,C} = 4\text{ns}$

We'll start by determining the functional specification for the system, expressing the result as a truth table which shows the value of the output S for the eight possible combinations of values for the P, Q, and R inputs. Given a particular set of input values, you can use the truth tables for the A, B, and C components to work your way through the circuit, from inputs to outputs. Please fill in the truth table below with the correct values for the S output:

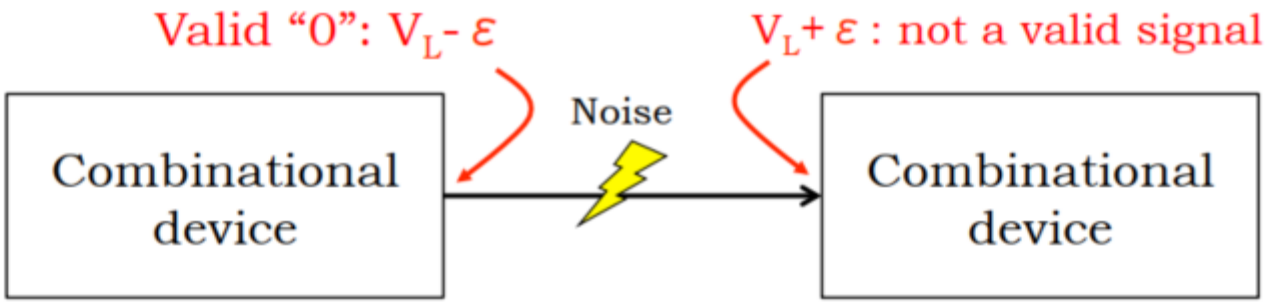
Example 2 (Cont.)

P	Q	R	S
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

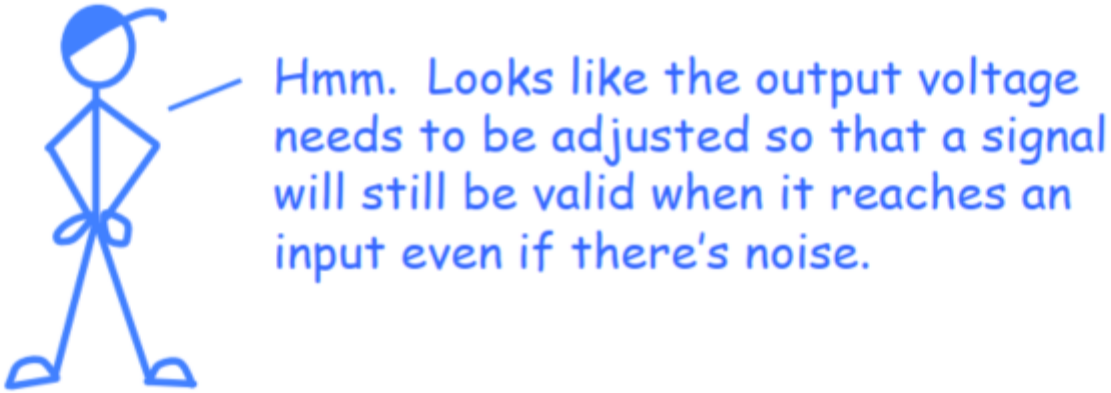
Finally, we need to derive the propagation delay, t_{PD}, of the system using the propagation delays of the components. To do this, consider all paths from the inputs (P, Q, R) to the outputs (S). For each path sum the propagation delays of the components along the path to compute how long it will take for a change in path's inputs to be reflected in the path's outputs. The system's propagation delay is the maximum of the path propagation delays. Please enter the system's propagation delay:

System t_{PD} in ns:

Noise On Combinational Systems

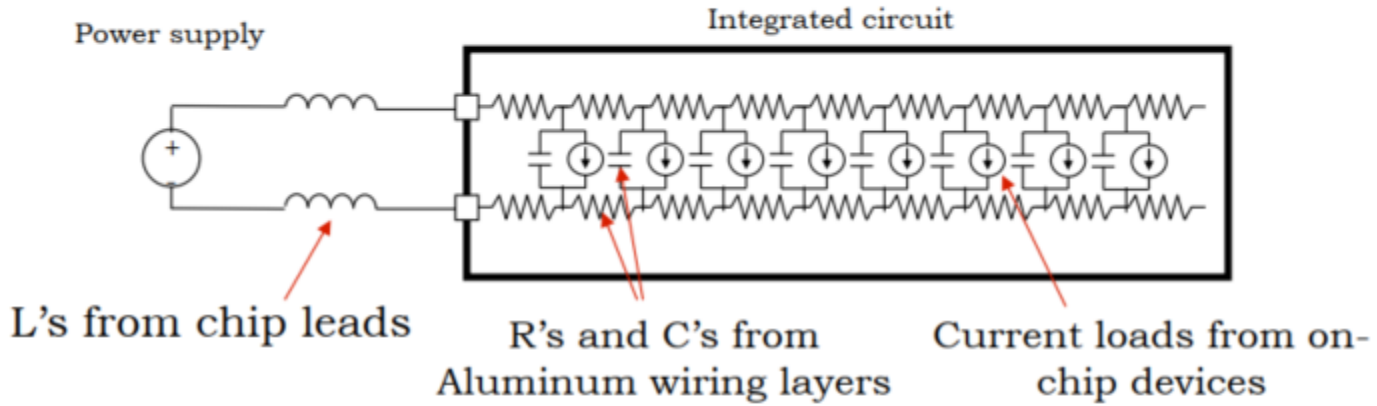


Upstream device transmits a signal at $V_L - \varepsilon$, a valid "0". Noise on the connecting wire causes the downstream device to receive $V_L + \varepsilon$, a signal in the forbidden zone.



Where Does Noise Come From?

- Parasitic resistance, inductance, capacitance
  - IR drop, L(dI/dt) drop, LC ringing from current steps

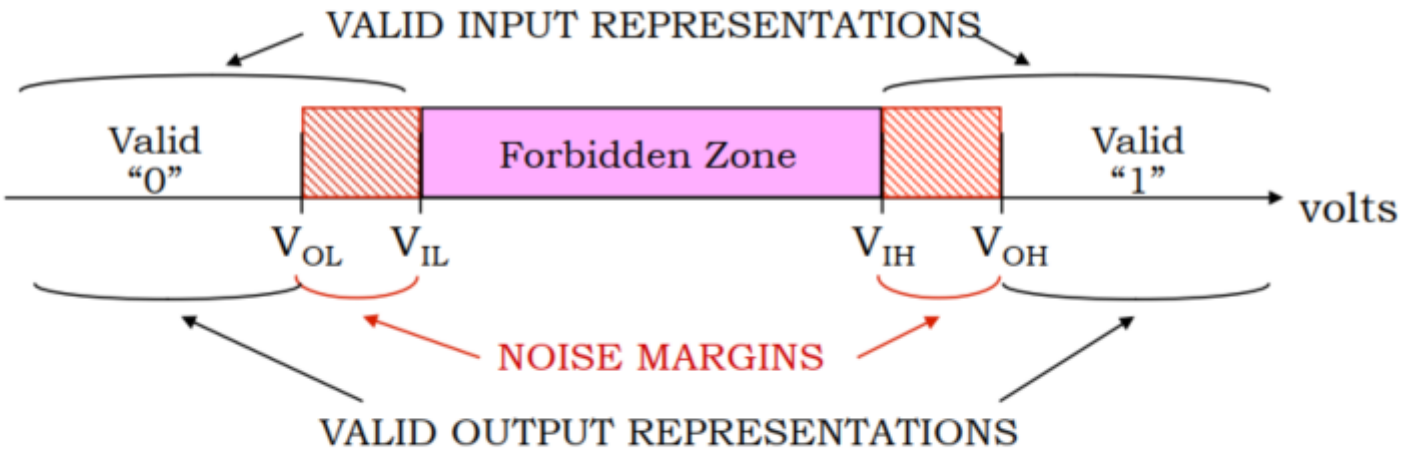


- Imprecision of component values
  - Manufacturing variations, allowable tolerances
- Environmental effects
  - External EM fields, temperature variations, etc.
- …

Solution – Noise Margins

Proposed fix: separate specifications for inputs and outputs

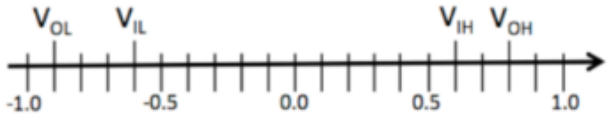
- digital output: "0" ≤ V_{OL}, "1" ≥ V_{OH}
- digital input: "0" ≤ V_{IL}, "1" ≥ V_{IH}
- $V_{OL} < V_{IL} < V_{IH} < V_{OH}$



A combinational device accepts marginal inputs and provides unquestionable outputs (to leave room for noise).

Example 3

A new family of logic devices uses signaling voltages in the range −1V to +1V. One proposed assignment of our voltage specification is shown below. Observe $V_{OL} = -0.9, V_{IL} = -0.6, V_{IH} = 0.6, V_{OH} = 0.8$.



The *noise immunity* of a signaling specification is the smaller of the two noise margins. What is the noise immunity for the signaling scheme proposed above? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell what the noise immunity is, write "NONE".

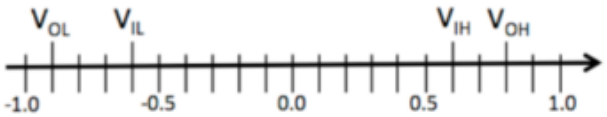
Noise immunity (V):

The output voltage of an inverter is measured to be 0.9V in the steady state. The inverter is a combinational device obeying the signaling specification shown above. What is the best characterization of the steady-state input voltage V_{IN} of the inverter when the measurement was made? Please give a numeric answer to the nearest .1 volt. If it is impossible to characterize V_{IN}, write "NONE".

$V_{IN}\,(V) <$

Solution 3

A new family of logic devices uses signaling voltages in the range −1V to +1V. One proposed assignment of our voltage specification is shown below. Observe $V_{OL} = -0.9, V_{IL} = -0.6, V_{IH} = 0.6, V_{OH} = 0.8$.



The *noise immunity* of a signaling specification is the smaller of the two noise margins. What is the noise immunity for the signaling scheme proposed above? Please give a numeric answer to the nearest .1 volt. If it is impossible to tell what the noise immunity is, write "NONE".

Noise immunity (V): **Answer:** 0.2

Explanation

The low noise margin is defined $V_{IL} - V_{OL}$. The high noise margin is defined as $V_{OH} - V_{IH}$. That means that the low noise margin is 0.3V and the high noise margin is 0.2V. Since noise immunity is defined as the smaller of the two noise margins, the noise immunity is 0.2 volts.

The output voltage of an inverter is measured to be 0.9V in the steady state. The inverter is a combinational device obeying the signaling specification shown above. What is the best characterization of the steady-state input voltage V_{IN} of the inverter when the measurement was made? Please give a numeric answer to the nearest .1 volt. If it is impossible to characterize V_{IN}, write "NONE".

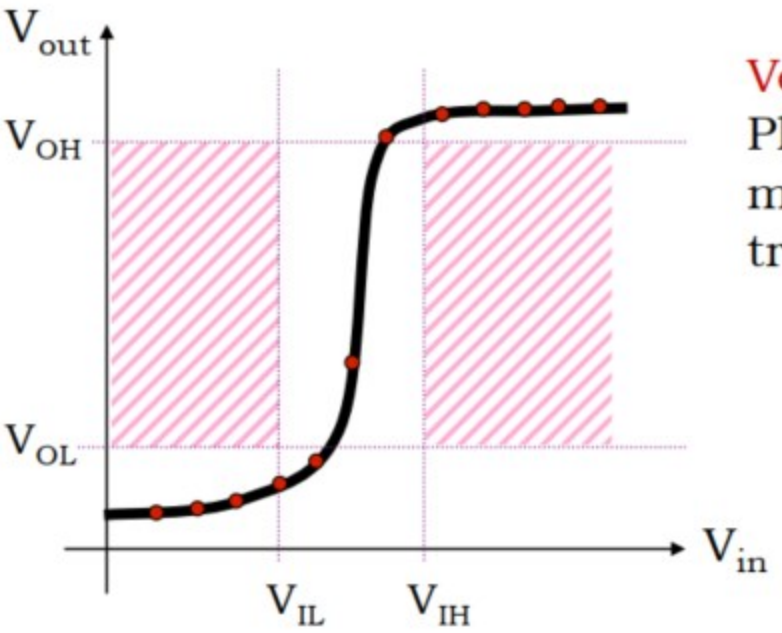
$V_{IN}\,(V) <$ **Answer:** 0.6

Explanation

A 0.9 volt output is a high output. If we are producing a high output, all we can definitively say about the input voltage is that it is not a valid high input because in that case, the output would be low. So the constraint on the input voltage is that $V_{IN} < 0.6V$. Note that you cannot assume that the input voltage is a valid low which would be less than -0.6V just because the output happens to be high. In other words, input voltages in the forbidden zone could produce a valid high output.

Simple Combinational Device – A Buffer

A simple *combinational device*: 0 → 0 1 → 1

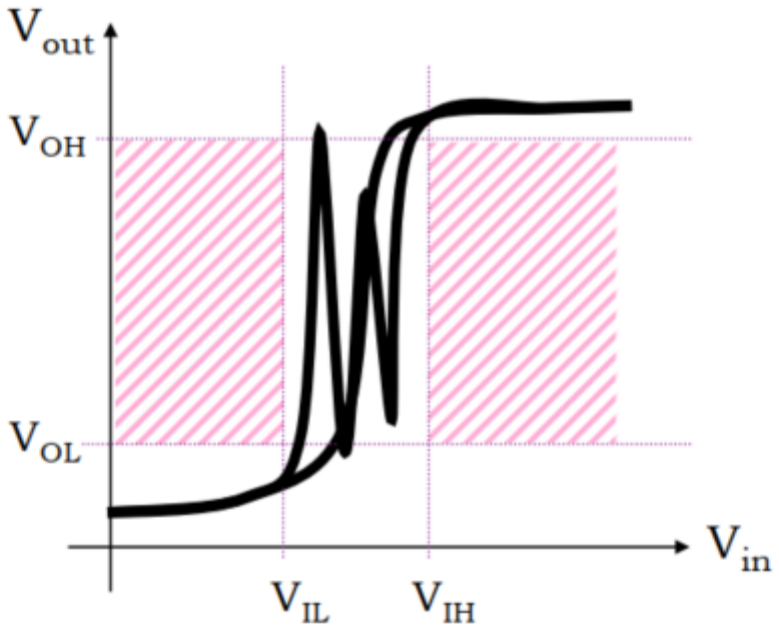


Voltage Transfer Characteristic (VTC): Plot of V_{out} vs. V_{in} where each measurement is taken after any transients have died out.

Note: VTC does not tell you anything about how fast a device is — it measures static behavior not dynamic behavior

Static Discipline requires that the VTC avoid the shaded regions (aka "*forbidden zones*"), which correspond to *valid* inputs but *invalid* outputs.

Voltage Transfer Characteristic



1) Note the VTC can do anything when $V_{IL} < V_{IN} < V_{IH}$.

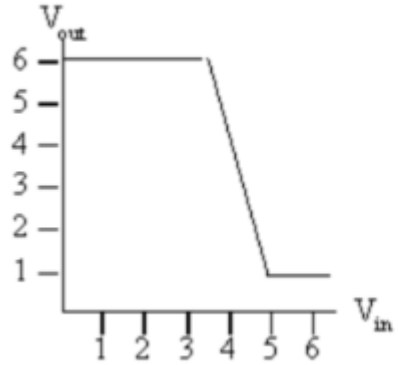
2) Note that the center white region is taller than it is wide (V_{OH}-V_{OL} > V_{IH}-V_{IL}). Net result: combinational devices must have GAIN > 1 and be NONLINEAR.

Example 3

As VP of Engineering at Inverters-R-Us, you've received the following four voltage transfer characteristics from your integrated circuit development lab. The goal is to decide which of the devices could be used as a combinational inverter with positive noise margins. In other words, the device obeys the static discipline and there are choices for V_{OL}, V_{IL}, V_{IH}, and V_{OH} for which $V_{IL} - V_{OL} > 0$ and $V_{OH} - V_{IH} > 0$.

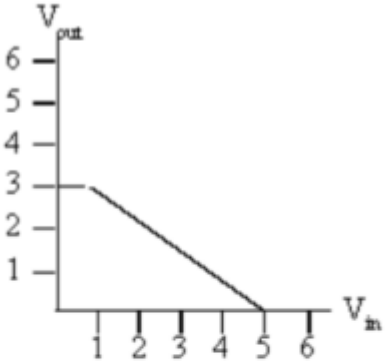
For each device, indicate whether it can be used as combinational inverter.

(A)

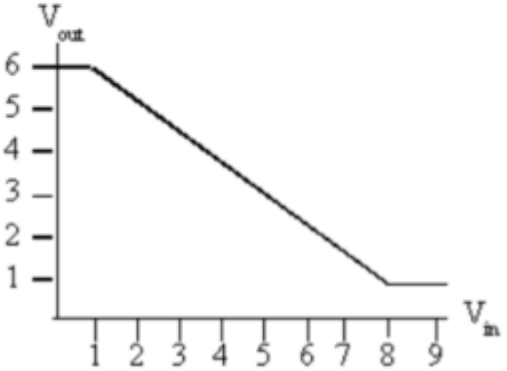


- Yes, usable :)
- No, not usable :(

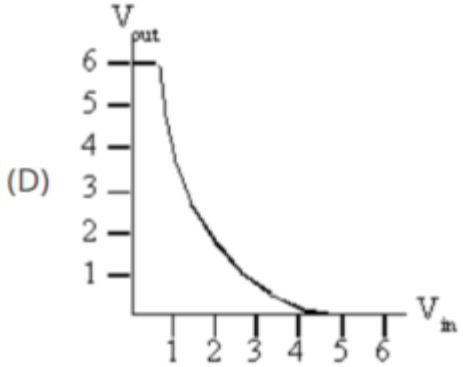
(B)



(C)



(D)



Solution 3

Explanation

Device A: $V_{OL} = 1V, V_{IL} = 3.5V, V_{IH} = 5V, V_{OH} = 6V$

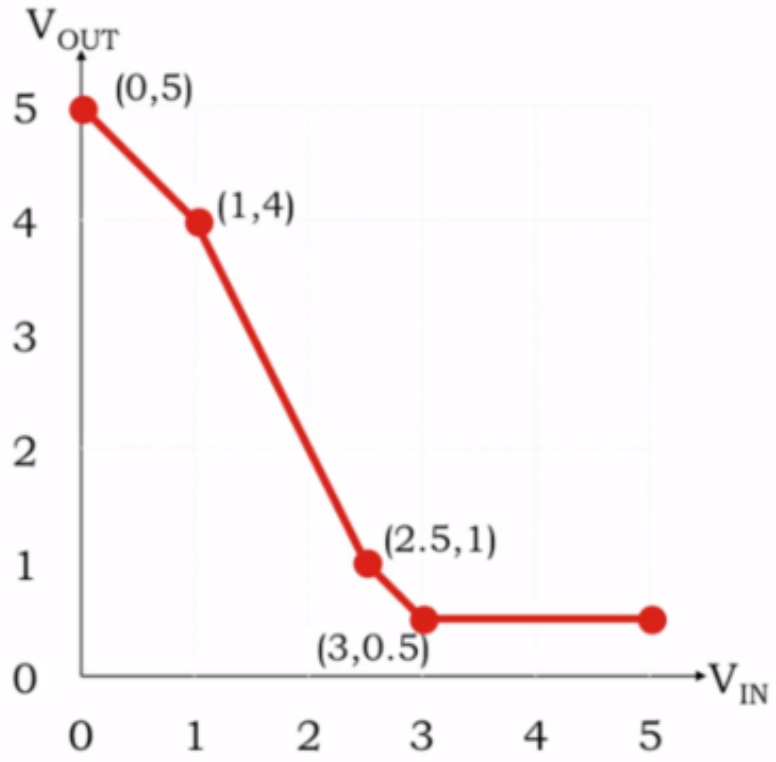
Device B: no values that would obey the static discipline exist, the gain is never greater than one

Device C: no values that would obey the static discipline exist, the gain is never greater than one

Device D: $V_{OL} = .5V, V_{IL} = 1V, V_{IH} = 3.5V, V_{OH} = 6V$

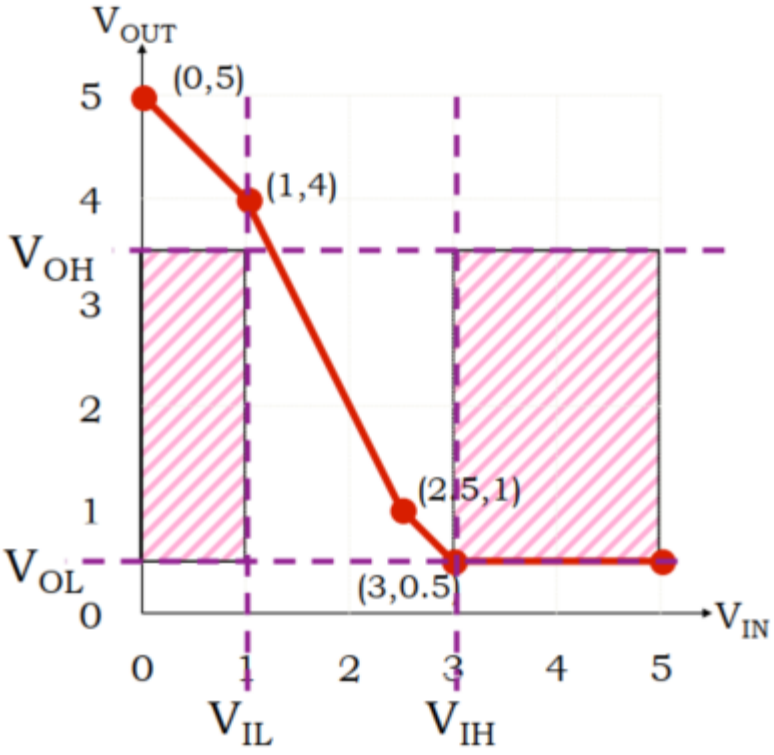
Can This Be a Combinational Inverter?

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification that would allow this device to be a combinational inverter?



Can This Be a Combinational Inverter?

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification that would allow this device to be a combinational inverter?



The device must be able to actually produce the desired output level. Thus, V_{OL} can be no lower than 0.5 V.

Try V_{OL} = 0.5 V

V_{IH} must be high enough to produce V_{OL}

Try V_{IH} = 3 V

Now, find noise margin N and compute

$V_{OH} = V_{IH} + N$

$V_{IL} = V_{OL} + N$

Then verify that $V_{OUT} \geq V_{OH}$ when $V_{IN} \leq V_{IL}$.

Try N = 0.5 V

Device is a combinational inverter when V_{OL}=0.5, V_{IL}=1, V_{IH}=3, V_{OH}=3.5

Processing Digital Signals – Boolean Logic

The binary representation has a natural correspondence to logic, and therefore digital circuits are commonly used to implement logic procedures.
For example, consider the logical "if" statement:

If X is TRUE AND Y is TRUE then Z is TRUE else Z is FALSE.

We can represent this statement using a boolean equation as:

$$Z = X \ AND \ Y$$

For brevity we often represent the AND function using

$$Z = X \cdot Y$$

Other Boolean Operators

The boolean equation for the statement:

If (A is TRUE) OR (B is NOT TRUE) then (C is TRUE) else (C is FALSE)

$$C = A + \bar{B}$$

The preceding equation contains two other useful functions. The OR function is represented using "+" and the NOT function using the bar symbol as in "$\bar{X}$" or the ~ symbol as in ~ *X*.

For example, we represent the condition "*B* is FALSE" as $\bar{B}$ or ~ *B*. We call $\bar{B}$, the complement of *B*.

OPERATOR	SYMBOL
AND	·
OR	+
NOT	~

Some logic operators and their symbols

Truth Table

We often find it convenient to use a *truth table* representation of boolean functions. A truth table enumerates all possible input value combinations and the corresponding output values.

For example, the truth table representation for $Z = X \cdot Y$ is

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Truth table for $Z = X \cdot Y$

$Z = X + Y$ is shown in

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

Truth table for $Z = X + Y$

$Z = \bar{X}$ is shown in

X	Z
0	1
1	0

Truth table for $Z = \bar{X}$

More Truth Tables

for $C = A + \bar{B}$ is shown in

A	B	C
0	0	1
0	1	0
1	0	1
1	1	1

Truth table for $C = A + \bar{B}$

The truth table for

$$\text{Output} = \overline{AB + C + D}$$

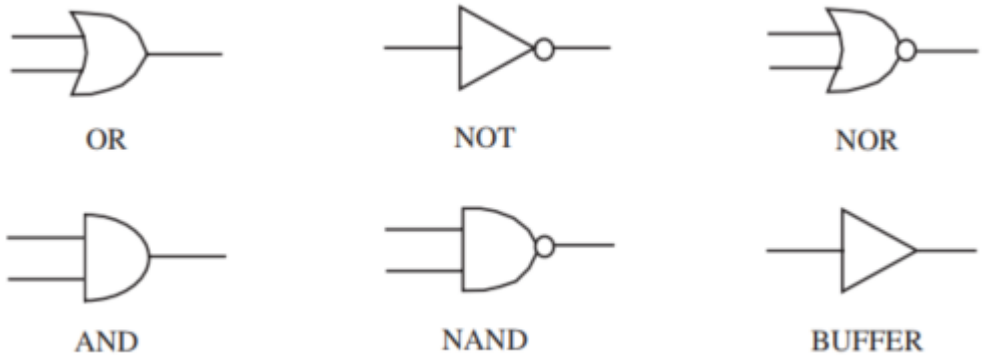
A	B	C	D	OUTPUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Combinational Gates Equivalent of Boolean Operators

Combinational gate abstraction

A combinational gate is an abstract representation of a circuit that satisfies two properties:

1. Its outputs are a function of its inputs alone.
2. It satisfies the static discipline.



Gate Symbols

For convenience, we often denote the *NOT* function in logic circuits using the "o" symbol. The buffer gate or identity gate simply copies the input value to its output, that is, $A = A$.

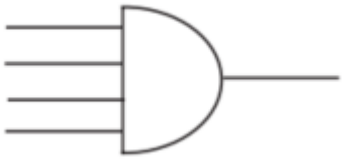
The *NAND* function is equivalent to the *AND* operation followed by the *NOT* operation. For example, $A = B$ NAND C is equivalent to $A = \overline{B \text{ AND } C}$. It is

Truth Table Of Basic Gates

INPUTS		AND	OR	NAND	NOR
B	C	$B \cdot C$	$B + C$	$\overline{B \cdot C}$	$\overline{B + C}$
0	0	0	0	1	1
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	0

Truth table for several two-input functions.

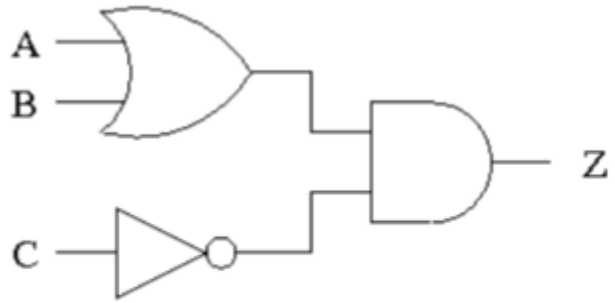
Gates can have multiple inputs. For example, we can have a four-input *AND* gate that implements the function $E = A \cdot B \cdot C \cdot D$ as shown in



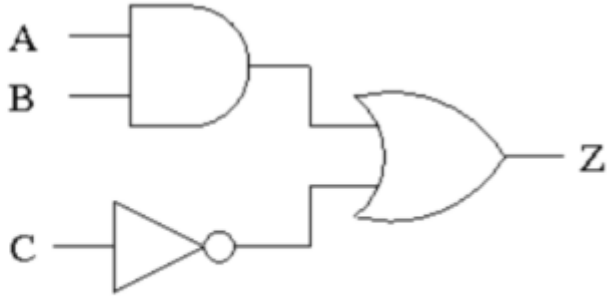
Four-Input AND

A four-input *AND* gate.

Example 4



Circuit 1



Circuit 2

A	B	C	Z
0	0	0	1
0	0	1	a
0	1	0	b
0	1	1	c
1	0	0	d
1	0	1	e
1	1	0	f
1	1	1	g

Which circuit satifies the truth table?

Find unknown a, f, d and b.

Solution 4

In the figure above there are two circuits and a partially filled in truth table. From the information in the truth table you can decide which circuit is described by that truth table. Enter the number of the chosen circuit:

2 ✔

What is the entry in the box labeled a?

0 ✔

What is the entry in the box labeled f?

1 ✔

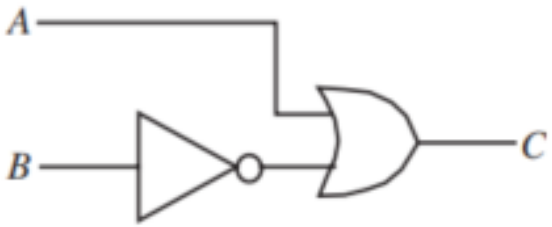
What is the entry in the box labeled d?

1 ✔

What is the entry in the box labeled b?

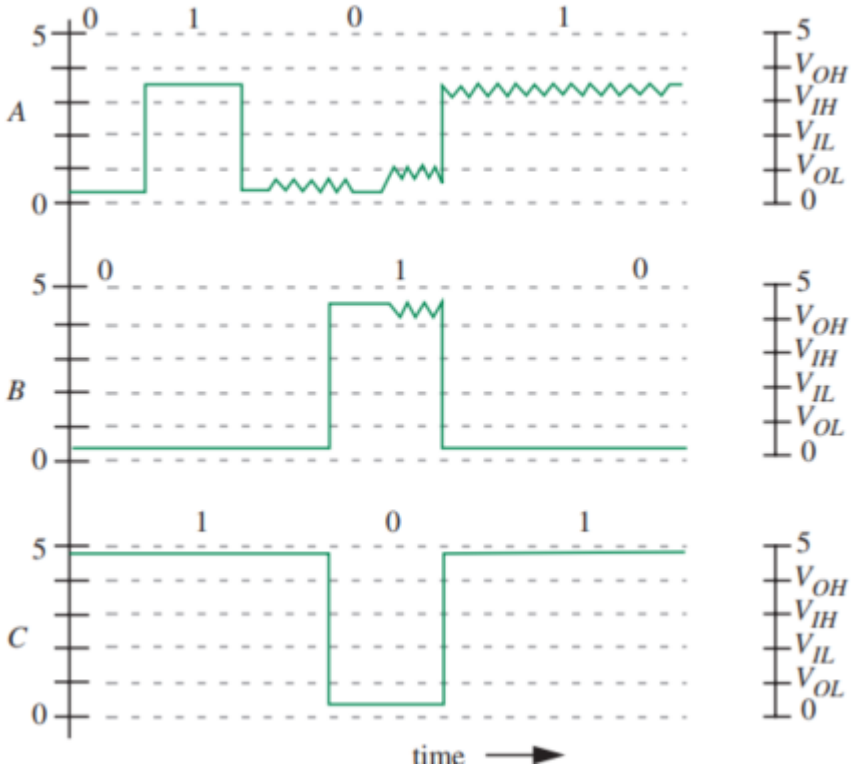
1 ✔

A Digital Circuit and Inputs



The gate-level digital circuit for $C = A + \overline{B}$.

has the following input-output relation, even in noise.



Demo – Chain Saw