## Microcontroller Based System Design

- This class is focused on the principles and practices of modern embedded systems design.
- In class, we will focus on computer architecture beyond the CPU, fundamentals of the hardware/software interface, techniques for sensing and controlling the physical world, and a few other topics.
- We will focus on the ARM Cortex-M3 (Acorn RISC (Reduced instruction set computing) Machine), FPGAs (Field Programmable Gate Array) and other supporting software, to learn how to build and program embedded systems.

#### 2019-2020 Fall 1

What is driving the embedded everywhere explosion?

#### Embedded, everywhere

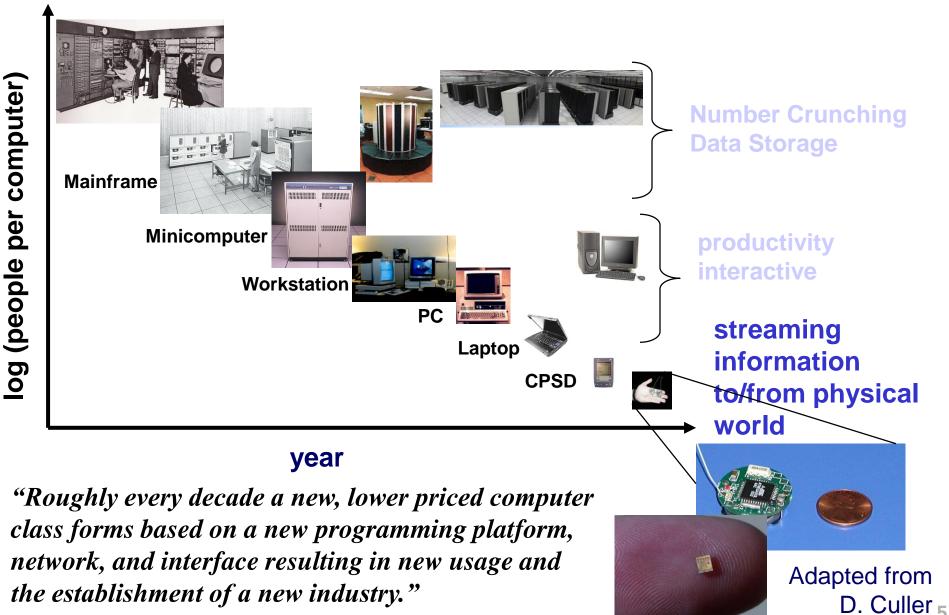


#### Outline

### Technology Trends

**Design Questions** 

## Bell's Law of Computer Classes: A new computing class roughly every decade



## Moore's Law: IC transistor count doubles every two years

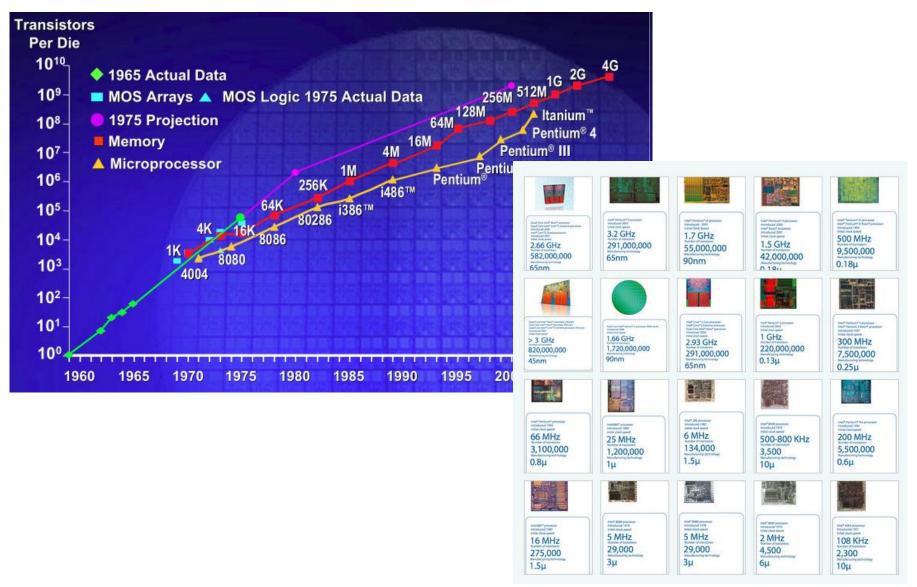


Photo Credit: Intel

#### Flash memory scaling: Rise of density & volumes; Fall (and rise) of prices

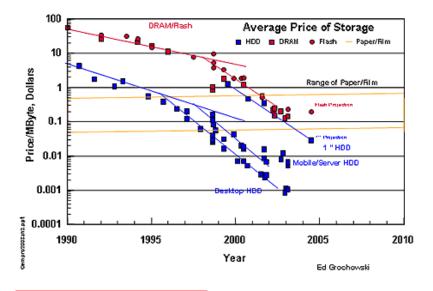
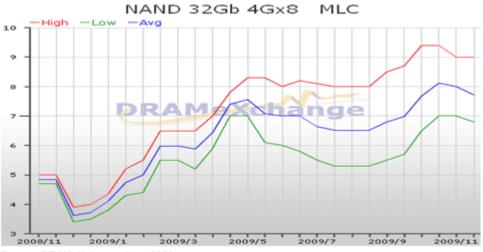
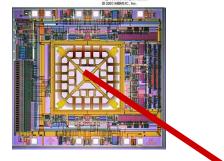


Figure-1 32Gb MLC NAND Flash contract price trend



Source: DRAMeXchange, Nov. 2009

## **MEMS Accelerometers:** Rapidly falling price and power

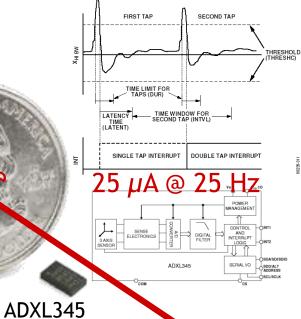


O(mA)





[Analog Devices, 2009]





## **Energy harvesting and storage:** Small doesn't mean powerless...

**1st Annual Workshop on** October 22, 2009 MICRO POWER TECHNOLOGIES

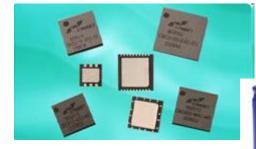
Radisson Hotel, San Jose, CA



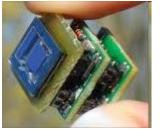


**RF** [Intel]

#### **Clare Solar Cell**

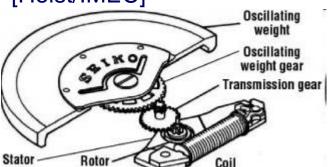


Thin-film batteries

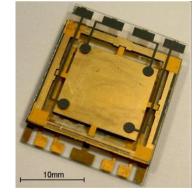


Piezoelectric [Holst/IMEC]





Coil

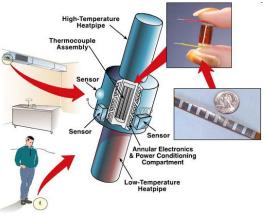


**Electrostatic Energy** Harvester [ICL]



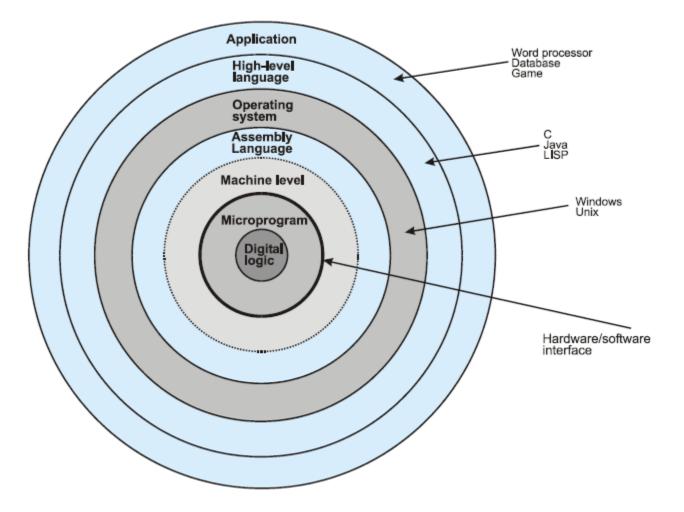


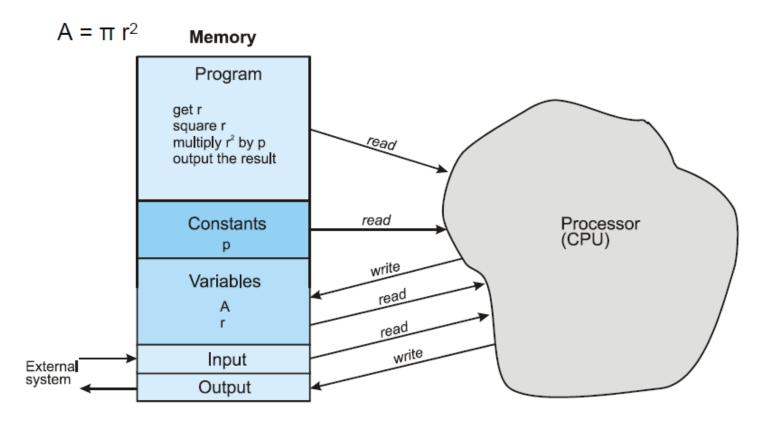
Shock Energy Harvesting **CEDRAT** Technologies



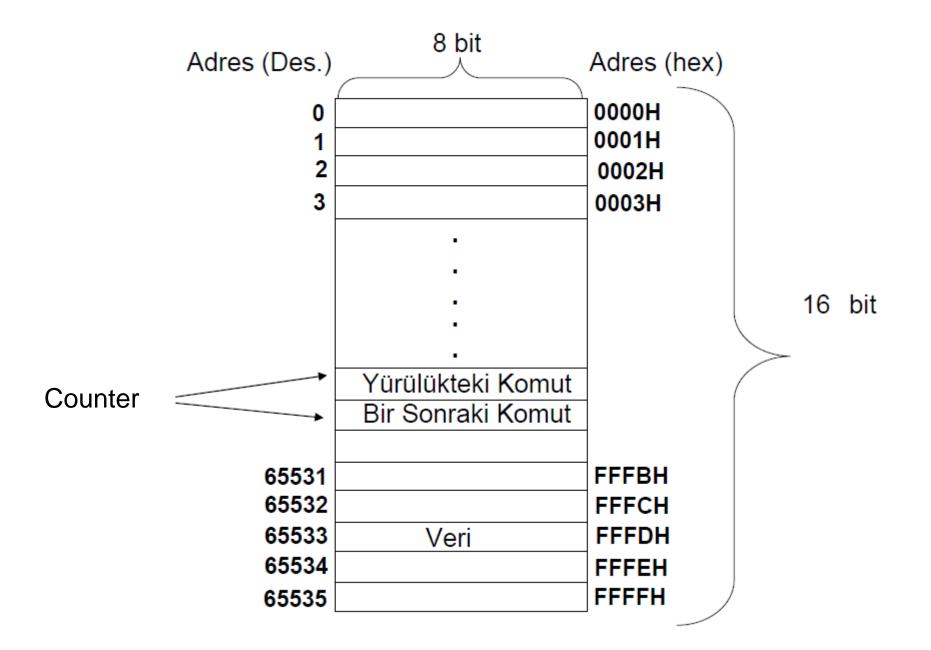
Thermoelectric Ambient Energy Harvester [PNNL]

#### **Machine Levels**



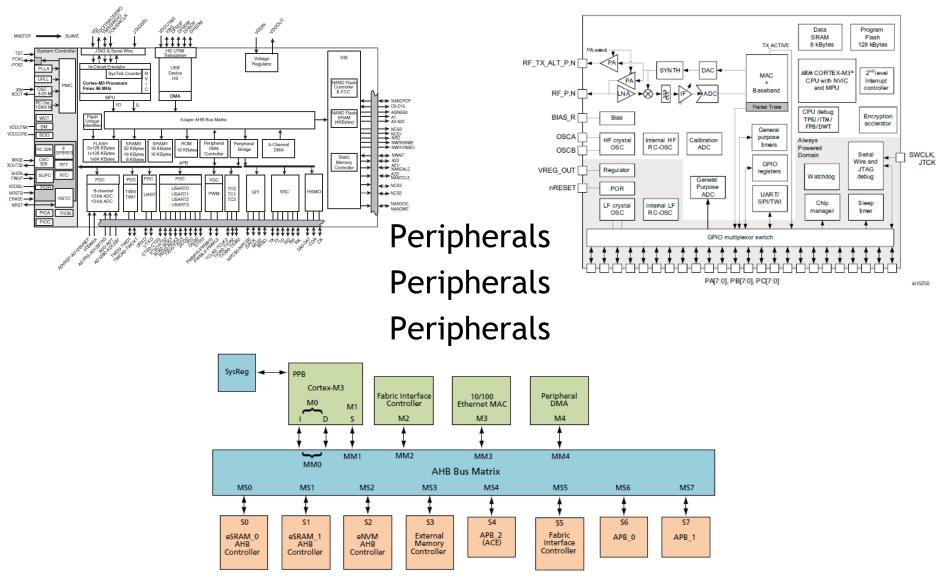


## Why study 32-bit MCUs and FPGAs?



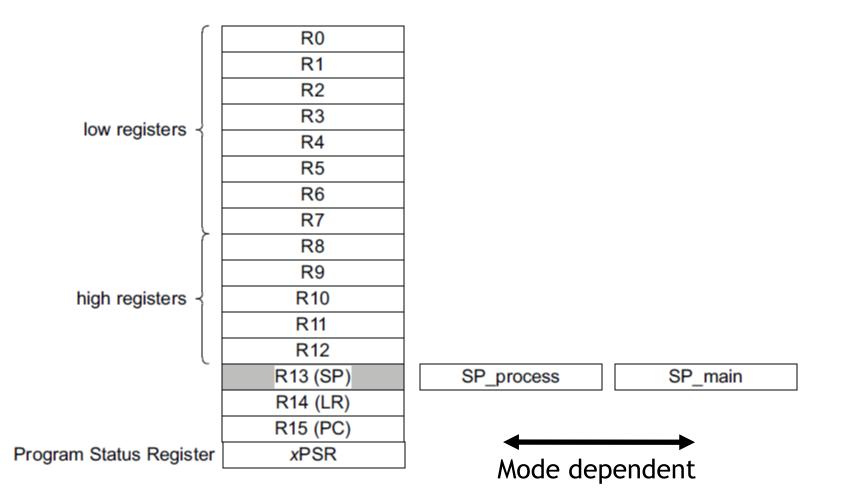
Why study the ARM architecture (and the Cortex-M3 in particular)? What differentiates these products from one another?

#### The difference is...



# Architecture

#### Registers



## Address Space

NE00FF000 0xE0042000 0xE0042000 0xE0040000         Rom Table External PPB         System         0xE0100000           0xE0040000 0xE0040000         ETM         Private peripheral bus - External         0xE004000           0xE0040000         Reserved         Private peripheral bus - Internal         0xE0040000           0xE000F000         SCS         External device         1.0GB           0xE000000         FPB         External device         1.0GB           0xE000000         ITM         0xA000000         0xA000000           0x44000000         ITM         0x4000000         0x4000000           0x42000000         IMB         Bit band alias         0x4000000         0x4000000           0x22000000         IMB         Bit band alias         0x4000000         0x4000000           0x22000000         IMB         Bit band alias         0x4000000         0x4000000           0x2000000         IMB         Bit band alias         0x2000000         0x4000000	0xE0100000			•			0xFFFFFFFF
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## Data processing instructions

Mnemonic	Instruction	Notes
ADC	Add with Carry	-
ADD	Add	Thumb permits use of a modified immediate constant or a zero-extended 12-bit immediate constant.
ADR	Form PC-relative Address	First operand is the PC. Second operand is an immediate constant. Thumb supports a zero-extended 12-bit immediate constant. Operation is an addition or a subtraction.
AND	Bitwise AND	-
BIC	Bitwise Bit Clear	-
CMN	Compare Negative	Sets flags. Like ADD but with no destination register.
CMP	Compare	Sets flags. Like SUB but with no destination register.
EOR	Bitwise Exclusive OR	-
MOV	Copies operand to destination	Has only one operand, with the same options as the second operand in most of these instructions. If the operand is a shifted register, the instruction is an LSL, LSR, ASR, or ROR instruction instead. See <i>Shift instructions</i> on page A4-10 for details. Thumb permits use of a modified immediate constant or a zero-extended 16-bit immediate constant.

#### Table A4-2 Standard data-processing instructions

#### **Application Program Status Register (APSR)**

31	30	29	28 3	27 2	26	0
N	z	С	v	Q	RESERVED	

APSR bit fields are in the following two categories:

- Reserved bits are allocated to system features or are available for future expansion. Further
  information on currently allocated reserved bits is available in *The special-purpose program status
  registers (xPSR)* on page B1-8. Application level software must ignore values read from reserved bits,
  and preserve their value on a write. The bits are defined as UNK/SBZP.
- Flags that can be set by many instructions:
  - N, bit [31] Negative condition code flag. Set to bit [31] of the result of the instruction. If the result is regarded as a two's complement signed integer, then N == 1 if the result is negative and N = 0 if it is positive or zero.
  - Z, bit [30] Zero condition code flag. Set to 1 if the result of the instruction is zero, and to 0 otherwise. A result of zero often indicates an equal result from a comparison.
  - C, bit [29] Carry condition code flag. Set to 1 if the instruction results in a carry condition, for example an unsigned overflow on an addition.
  - V, bit [28] Overflow condition code flag. Set to 1 if the instruction results in an overflow condition, for example a signed overflow on an addition.
  - Q, bit [27] Set to 1 if an SSAT or USAT instruction changes (saturates) the input value for the signed or unsigned range of the result.