Electronic Devices and Circuit Theory

Boylestad

DC Biasing - BJTs

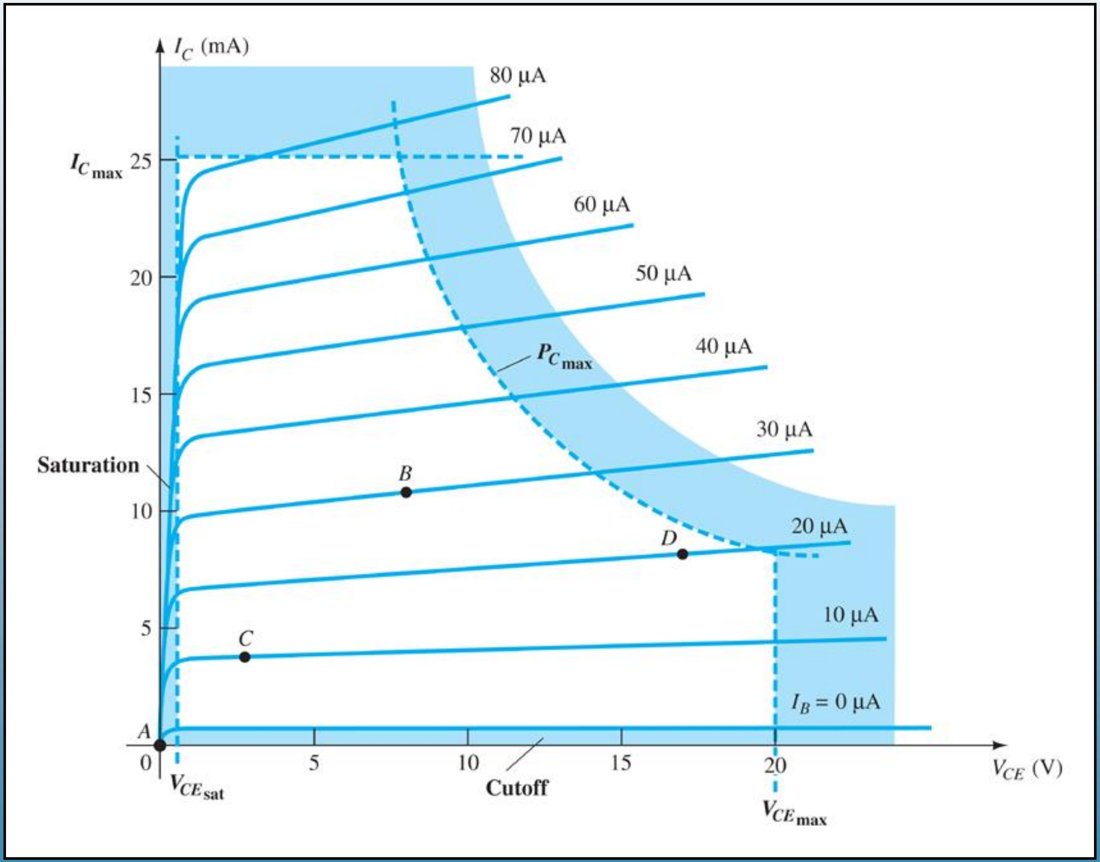
Chapter 4

Biasing

Biasing: Applying DC voltages to a transistor in order to turn it on so that it can amplify AC signals.

Operating Point

The DC input establishes an operating or *quiescent point* called the ***Q-point***.



The Three Operating Regions

Active or Linear Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is reverse biased

Cutoff Region Operation

- Base–Emitter junction is reverse biased

Saturation Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is forward biased

DC Biasing Circuits

Fixed-bias circuit

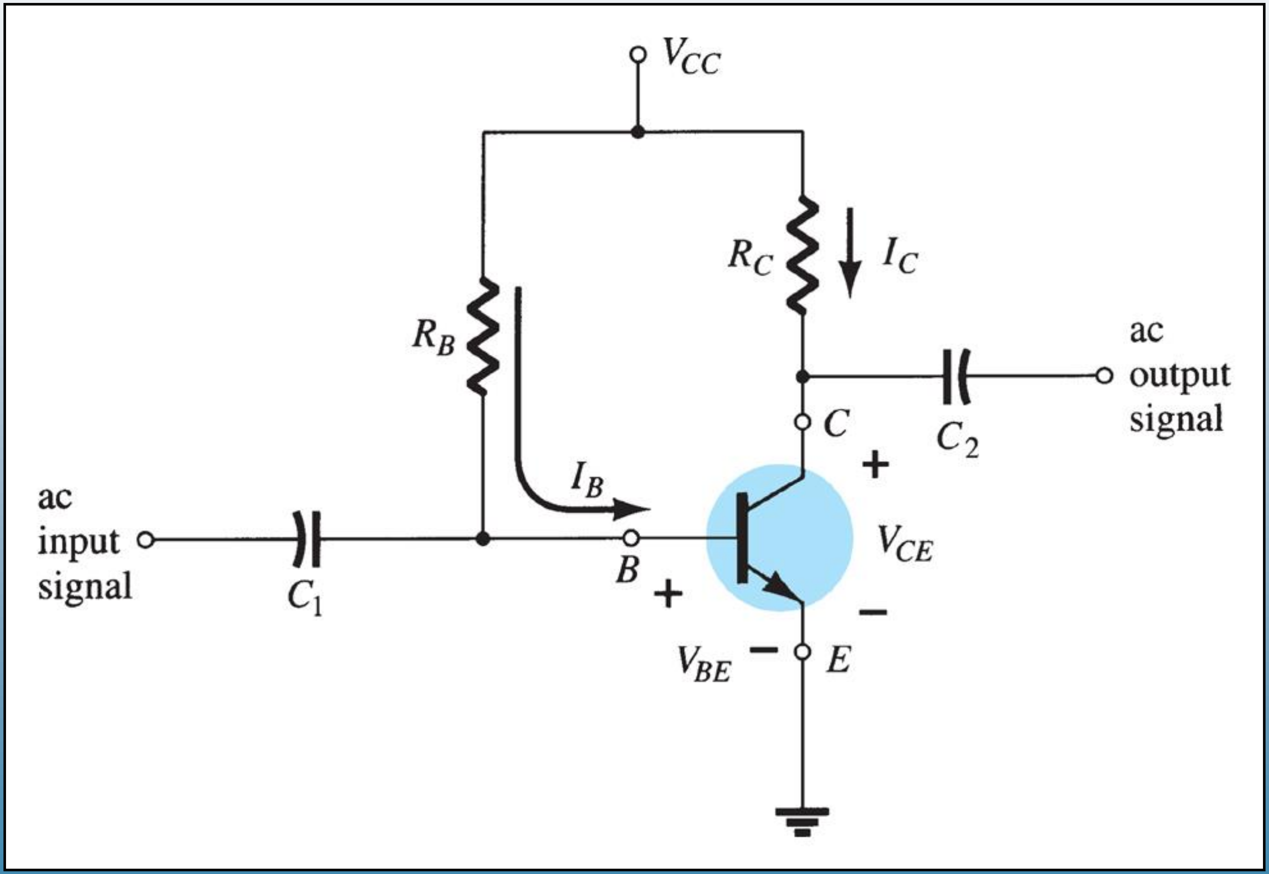
Emitter-stabilized bias circuit

Collector-emitter loop

Voltage divider bias circuit

DC bias with voltage feedback

Fixed Bias


V_{CC}
R_C
I_C
R_B
ac
output
signal
C
C_2
I_B
+
ac
input
signal
V_{CE}
B
+
C_1
−
V_{BE}
−
E

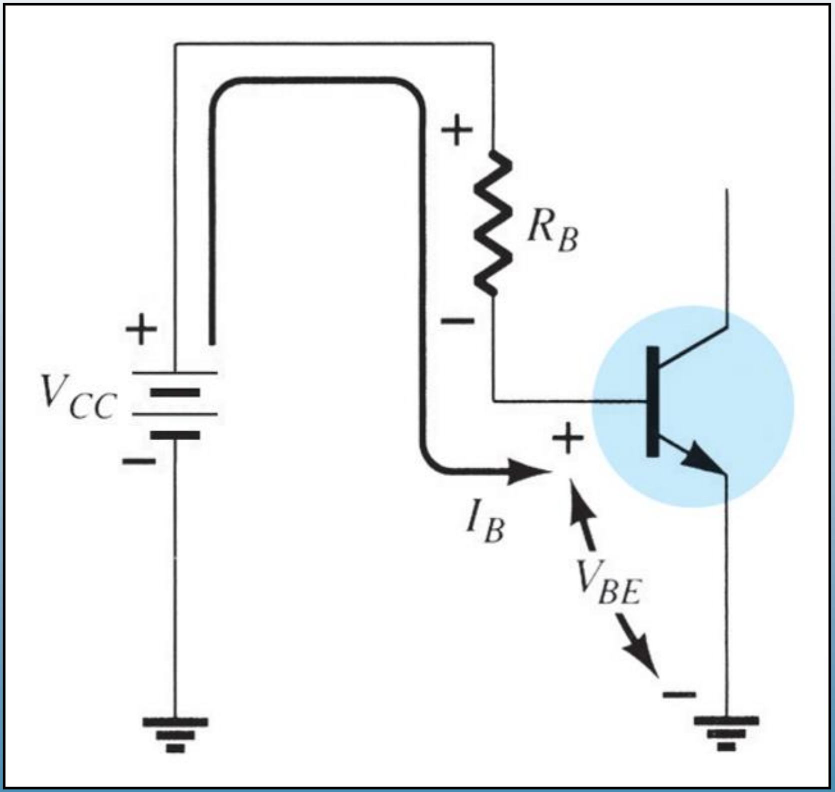
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



Collector-Emitter Loop

Collector current:

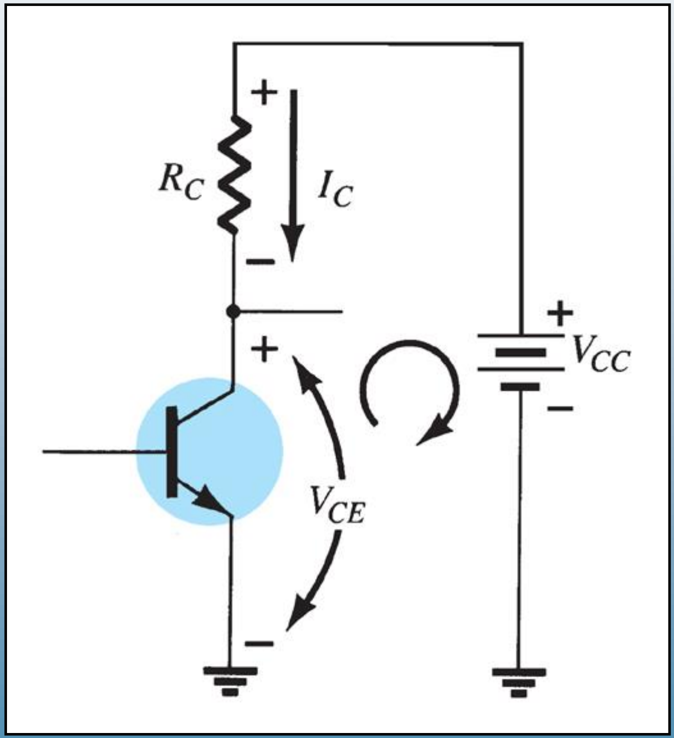
$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

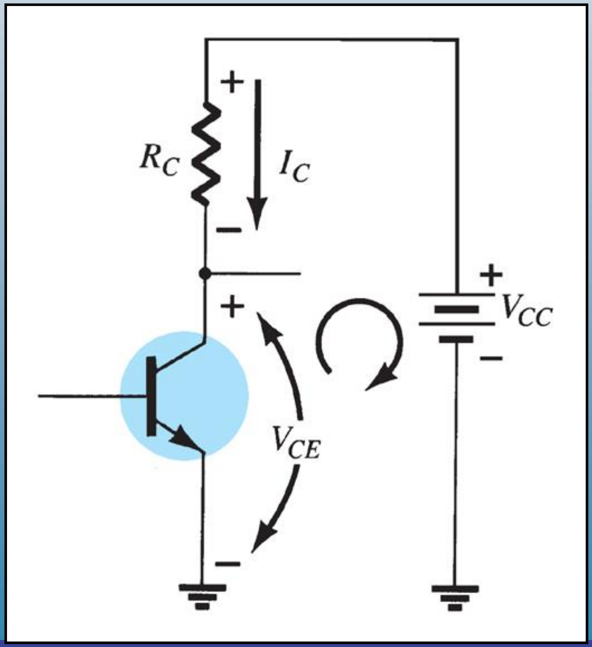


Saturation

When the transistor is operating in **saturation**, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\ V$$



Load Line Analysis

The load line end points are:

I_{csat}

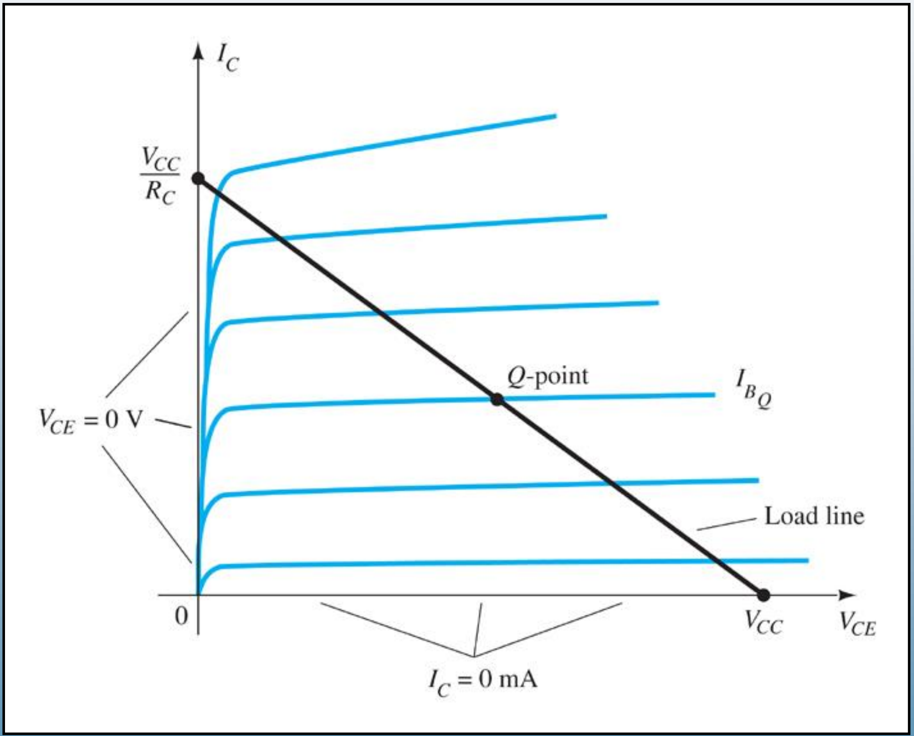
$V_{CE} = 0\text{ V}$

$I_C = V_{CC} / R_C$

$V_{CEcutoff}$

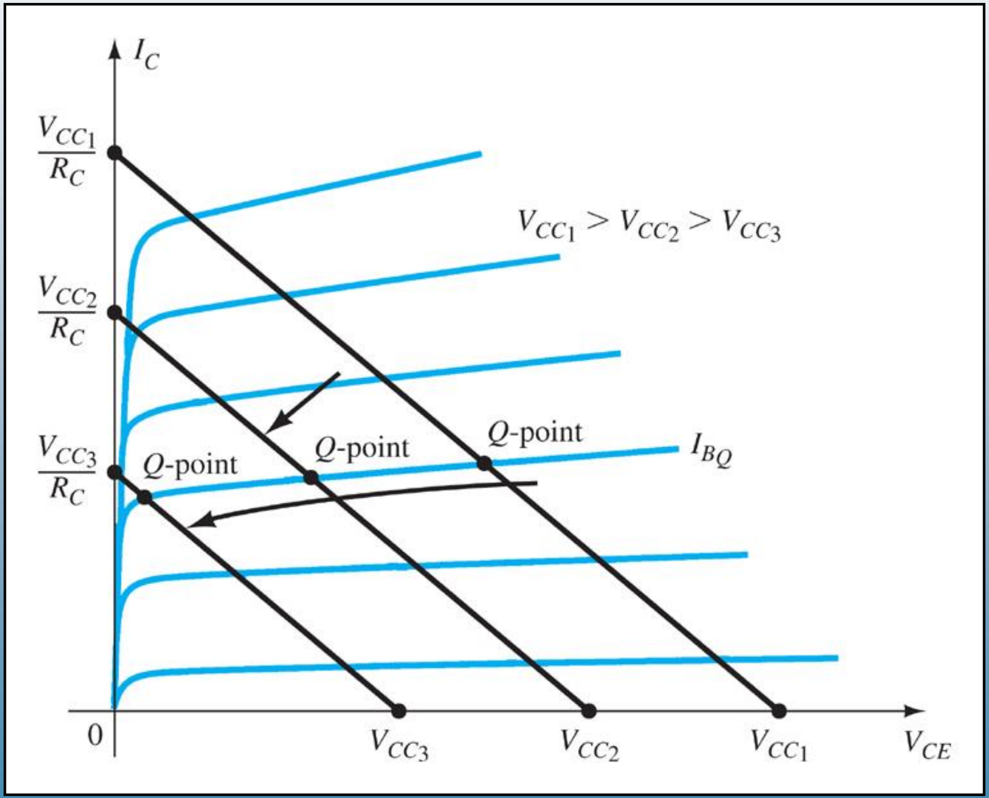
$I_C = 0\text{ mA}$

$V_{CE} = V_{CC}$

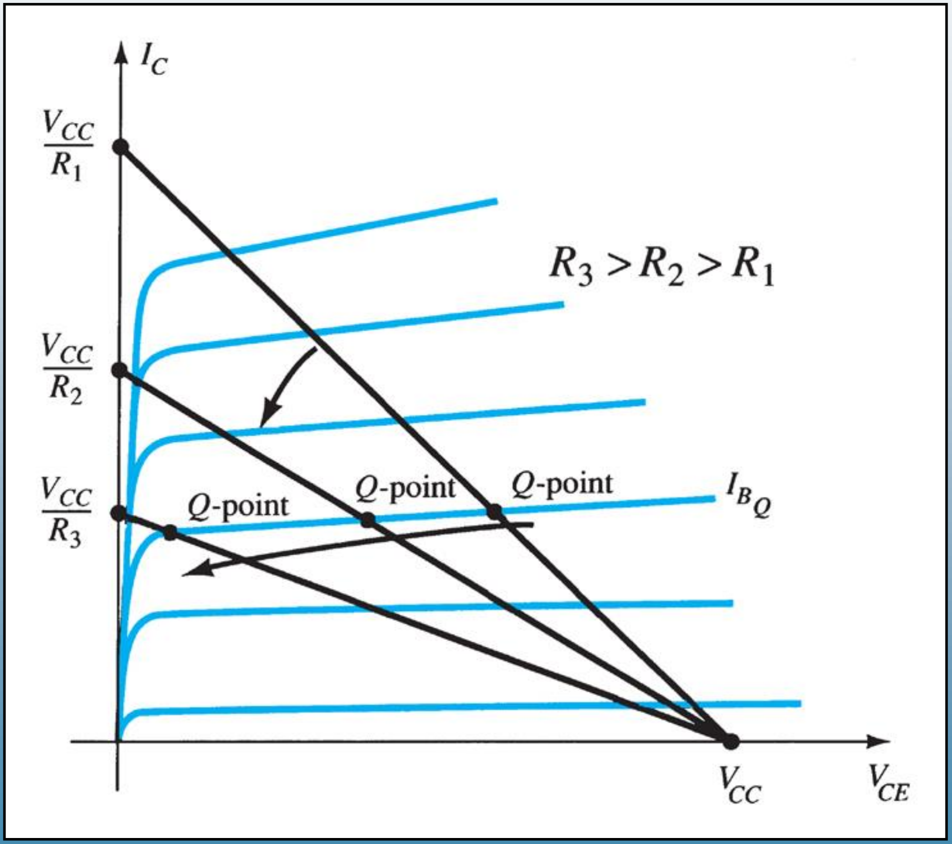


The Q-point is the operating point where the value of R_B sets the value of I_B that controls the values of V_{CE} and I_C.

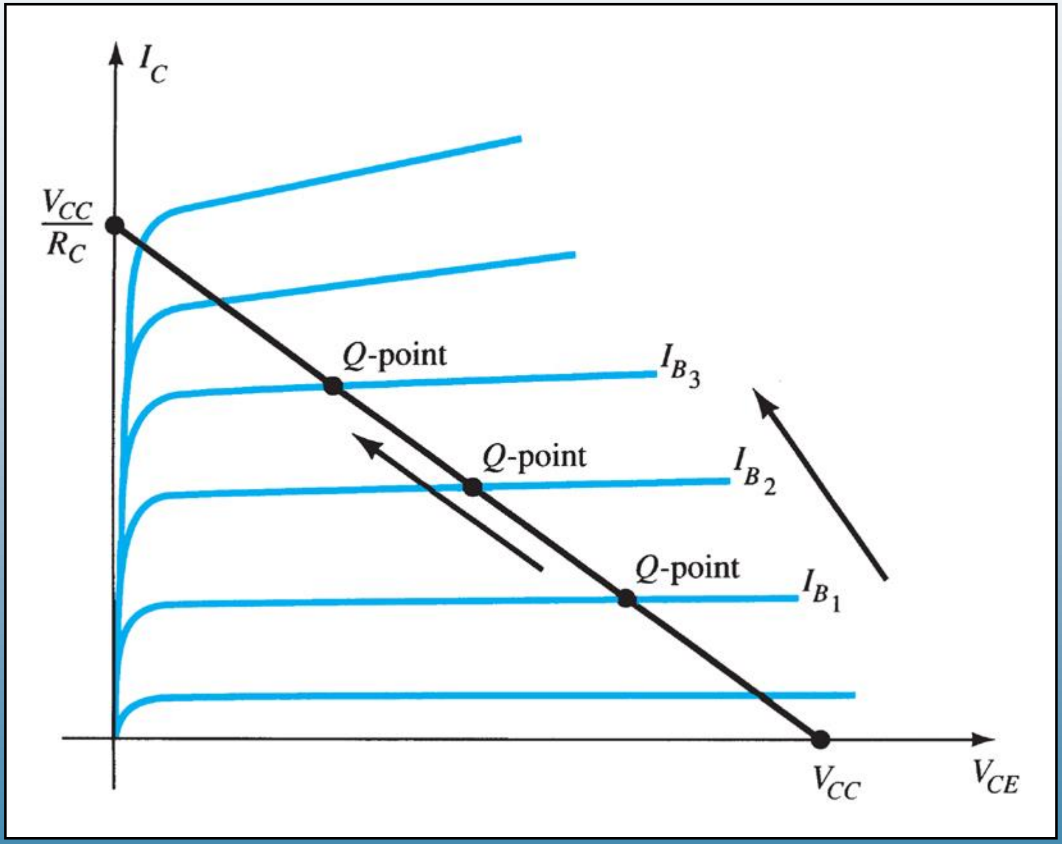
The Effect of V_{CC} on the Q-Point



The Effect of R_C on the Q-Point

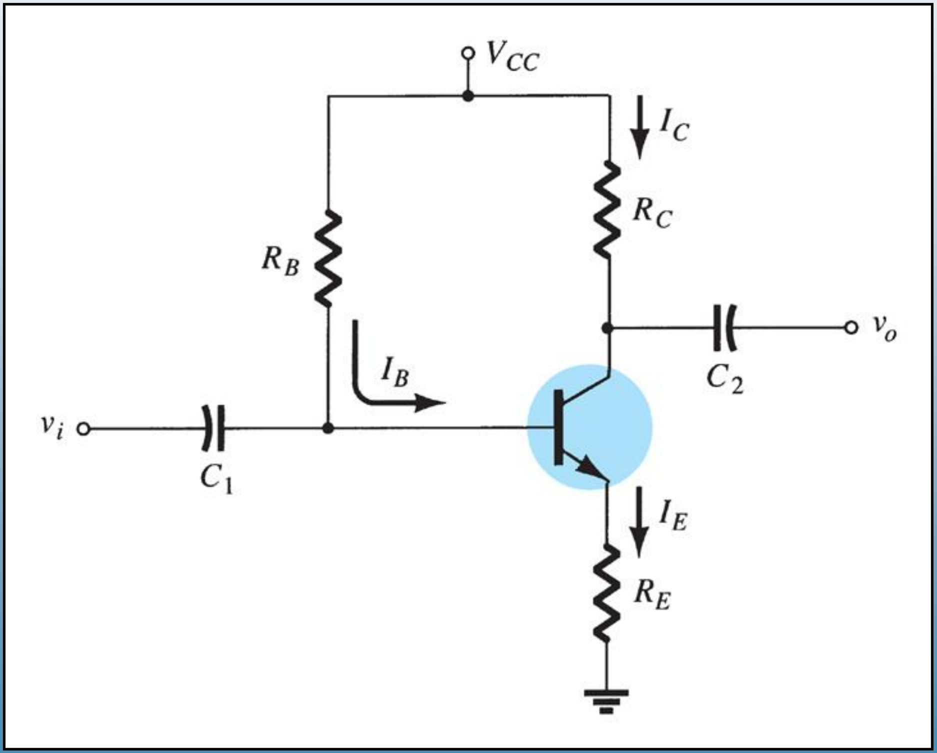


The Effect of I_B on the Q-Point



Emitter-Stabilized Bias Circuit

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

From Kirchhoff's voltage law:

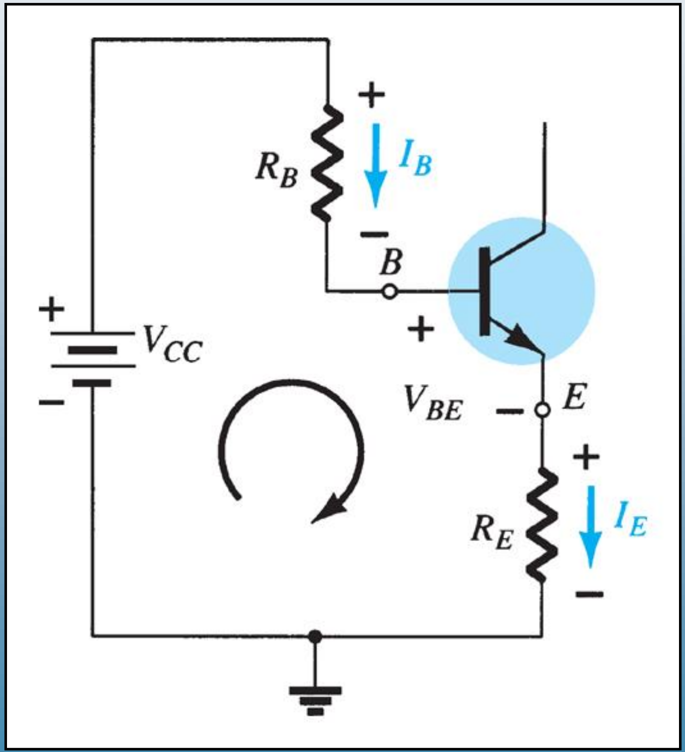
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

From Kirchhoff's voltage law:

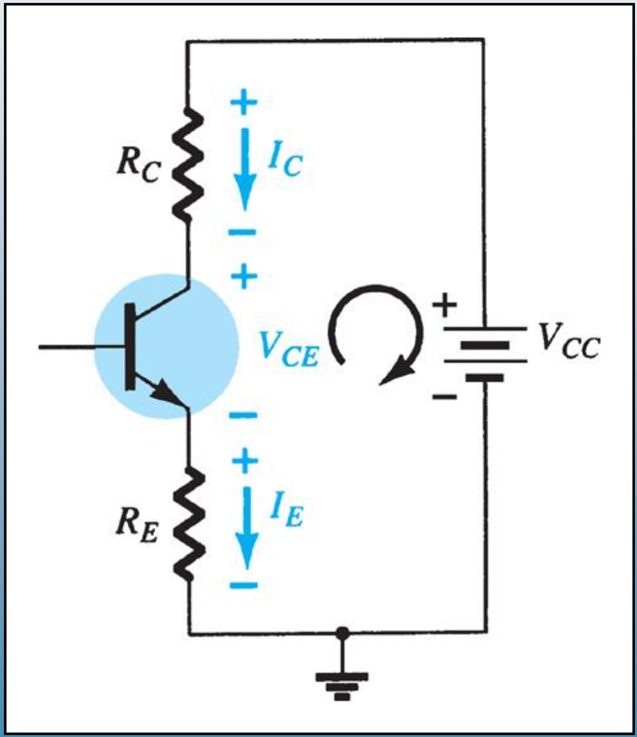
$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Also:

$$V_E = I_E R_E$$
$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$
$$V_B = V_{BE} + V_E$$

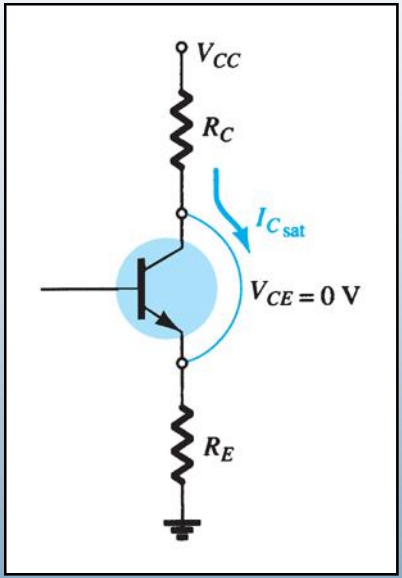


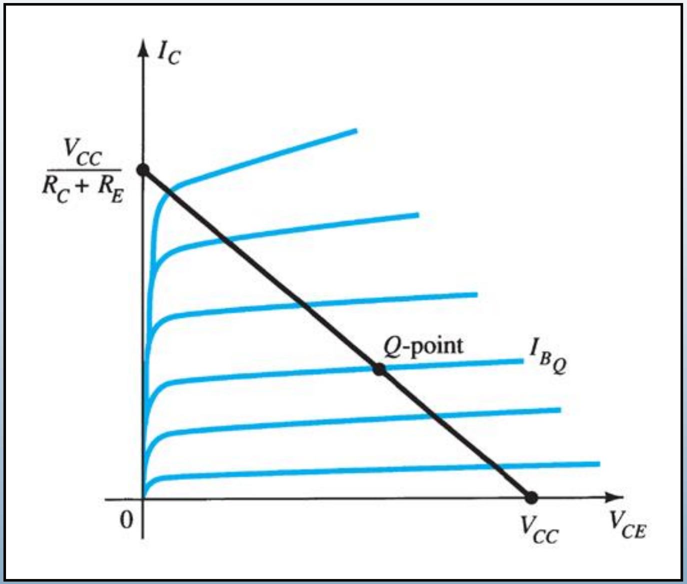
Improved Biased Stability

Stability refers to a condition in which the currents and voltages remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding R_E to the emitter improves the stability of a transistor.

Saturation Level





The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$I_C = 0 \text{ mA}$$
$$V_{CE} = V_{CC}$$

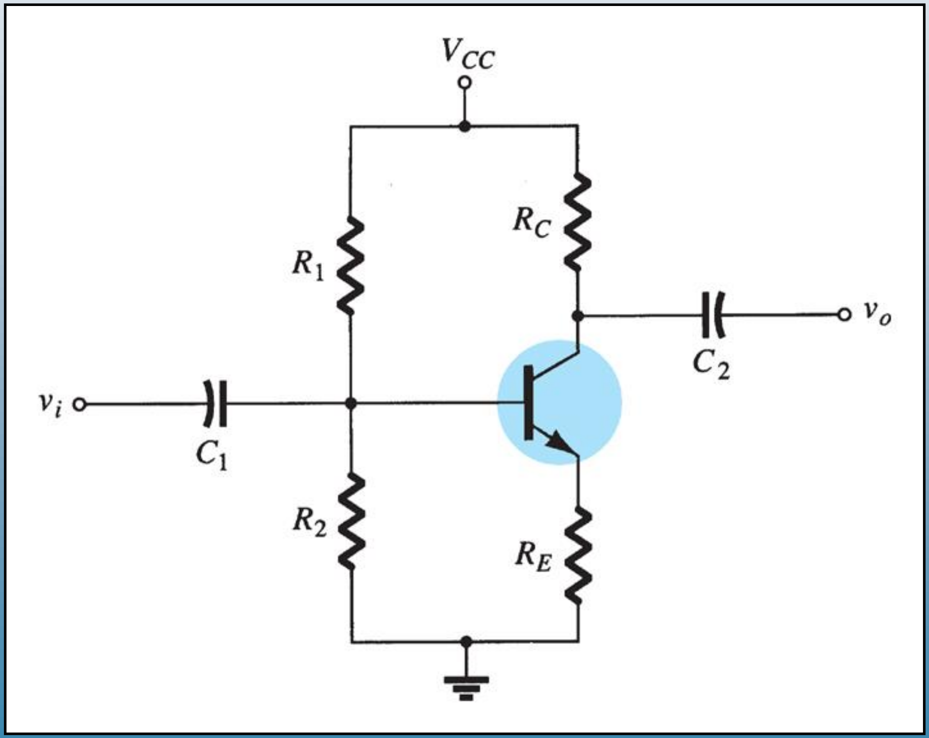
I_{Csat}:

$$V_{CE} = 0 \text{ V}$$
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β.



Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

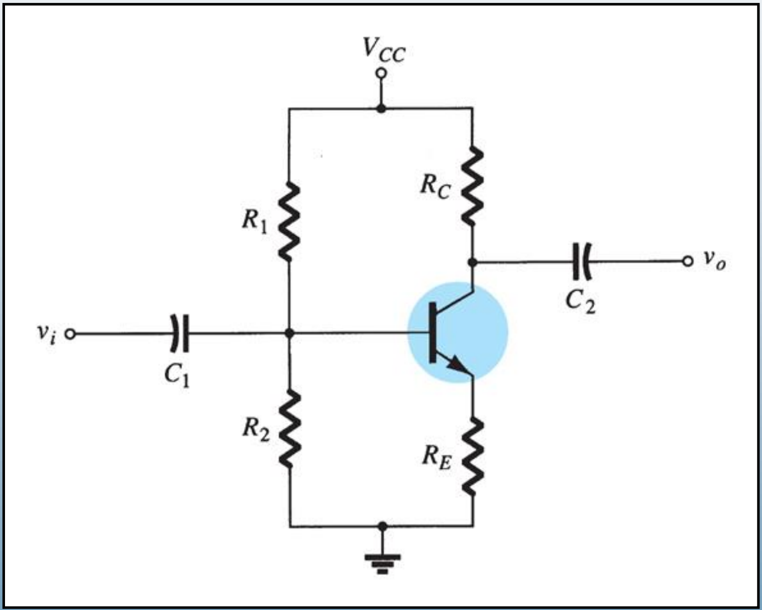
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$V_{BE} = V_B - V_E$$

0.7

$$I_E = \frac{V_E}{R_E}$$



From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\,\text{mA}$$

Saturation:

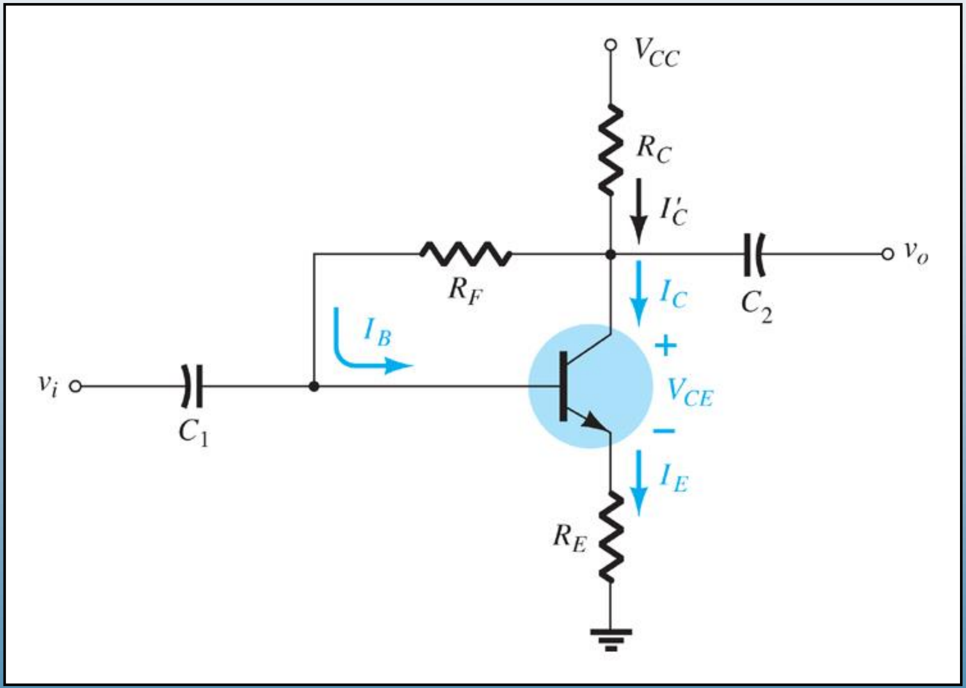
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\,\text{V}$$

DC Bias With Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

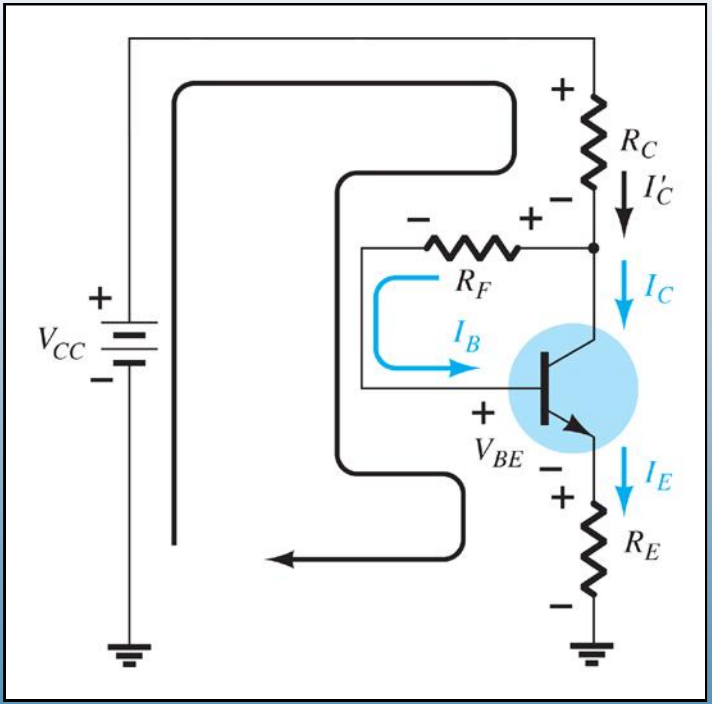
In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$



Where $I_B << I_C$:

$$I'_C = I_C + I_B \cong I_C$$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

Collector-Emitter Loop

Applying Kirchoff's voltage law:

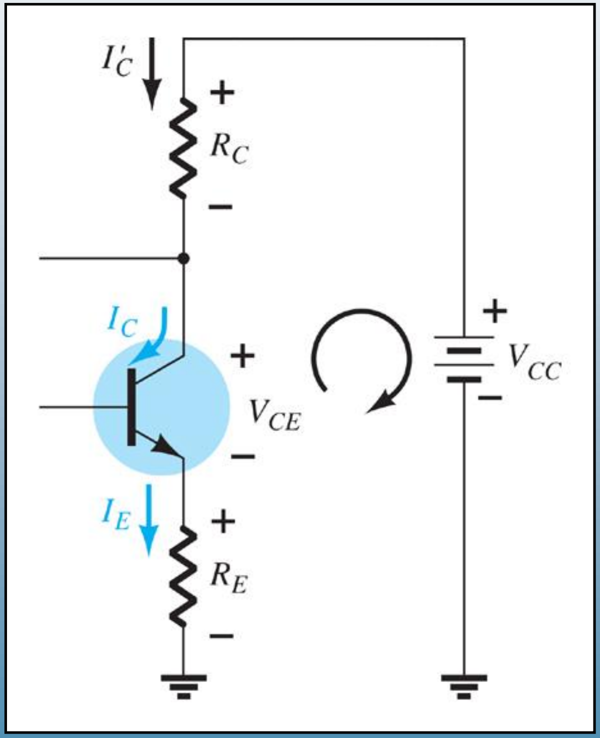
$$R_E I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff

$$V_{CE} = V_{CC}$$

$$I_C = 0\,mA$$

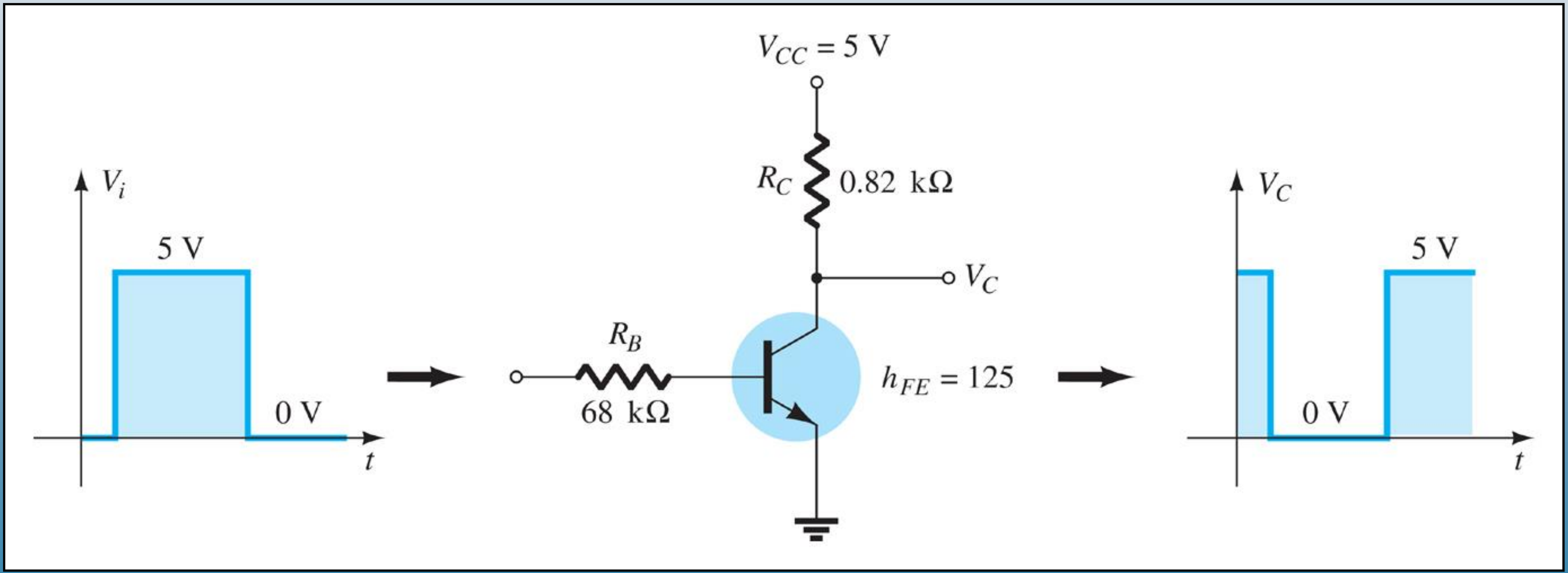
Saturation

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\,V$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



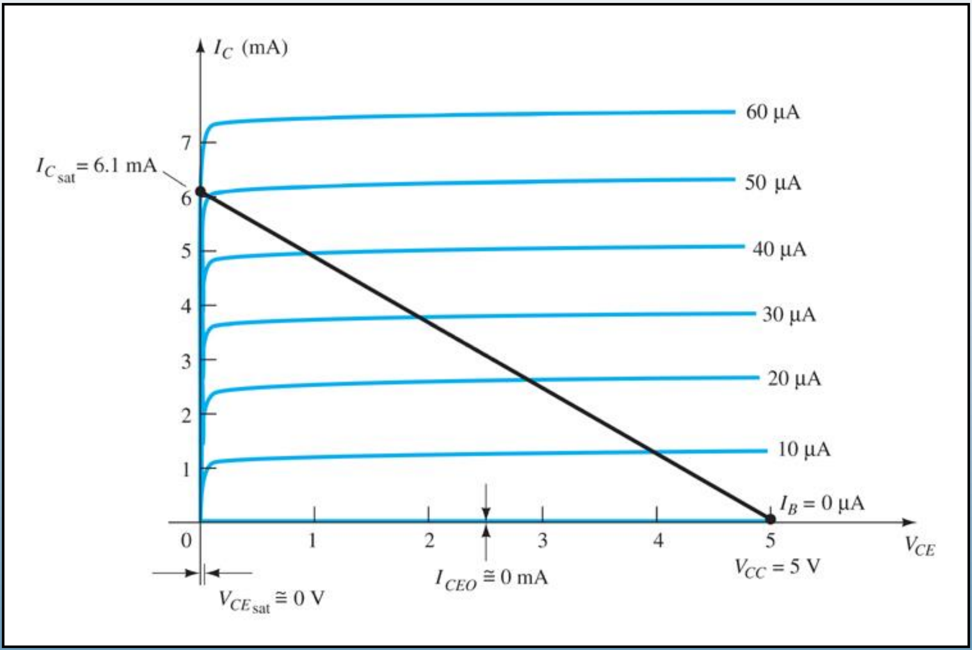
Switching Circuit Calculations

Saturation current:

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$



Emitter-collector resistance at saturation and cutoff:

$$R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$$

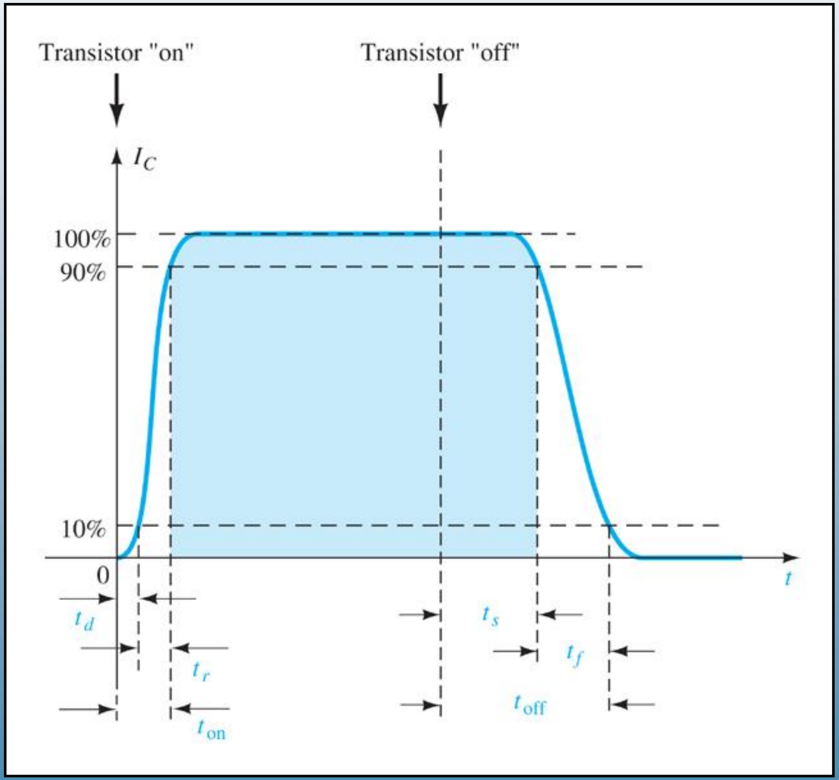
$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$

Switching Time

Transistor switching times:

$$t_{on} = t_r + t_d$$

$$t_{off} = t_s + t_f$$



Troubleshooting Hints

Approximate voltages

$V_{BE} \cong 0.7$ V for silicon transistors

$V_{CE} \cong 25\%$ to 75% of V_{CC}

Test for opens and shorts with an ohmmeter.

Test the solder joints.

Test the transistor with a transistor tester or a curve tracer.

Note that the load or the next stage affects the transistor operation.

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.