BME2322 – Logic Design

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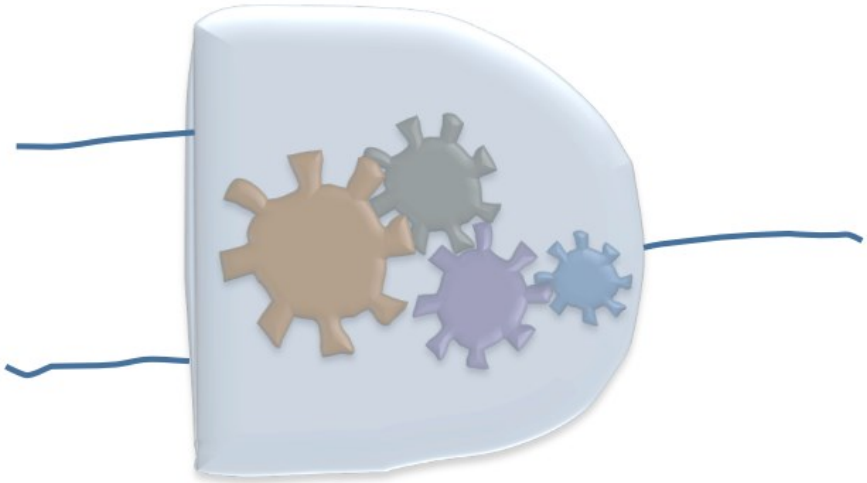
LECTURE 3

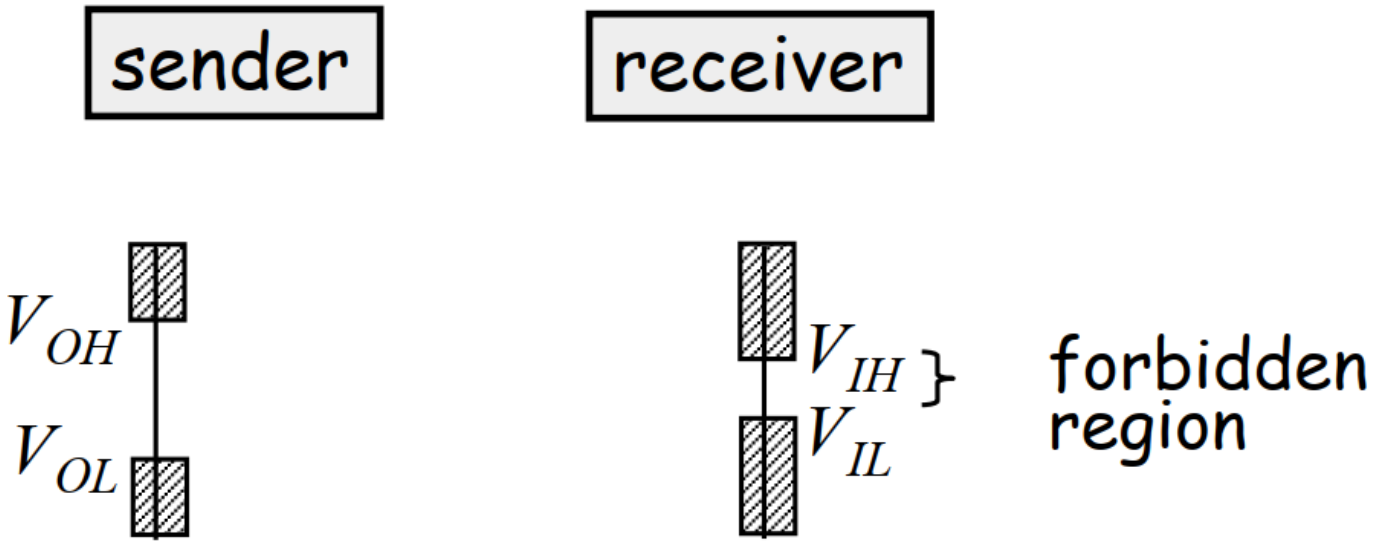
Inside the Digital Gates

Inside the Digital Gate



The Digital Abstraction

- Discretize value: 0, 1
- Static discipline -- digital devices meet voltage thresholds

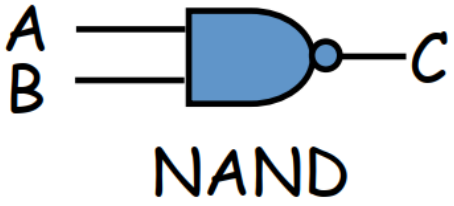


Specifies how gates must be designed

Combinational Elements

Combinational gate abstraction

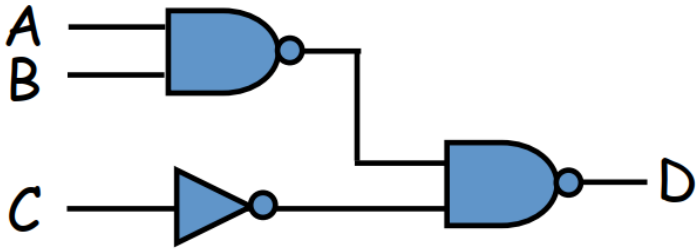
- outputs function of input alone
- satisfies static discipline



A	B	C
0	0	1
0	1	1
1	0	1
1	10	

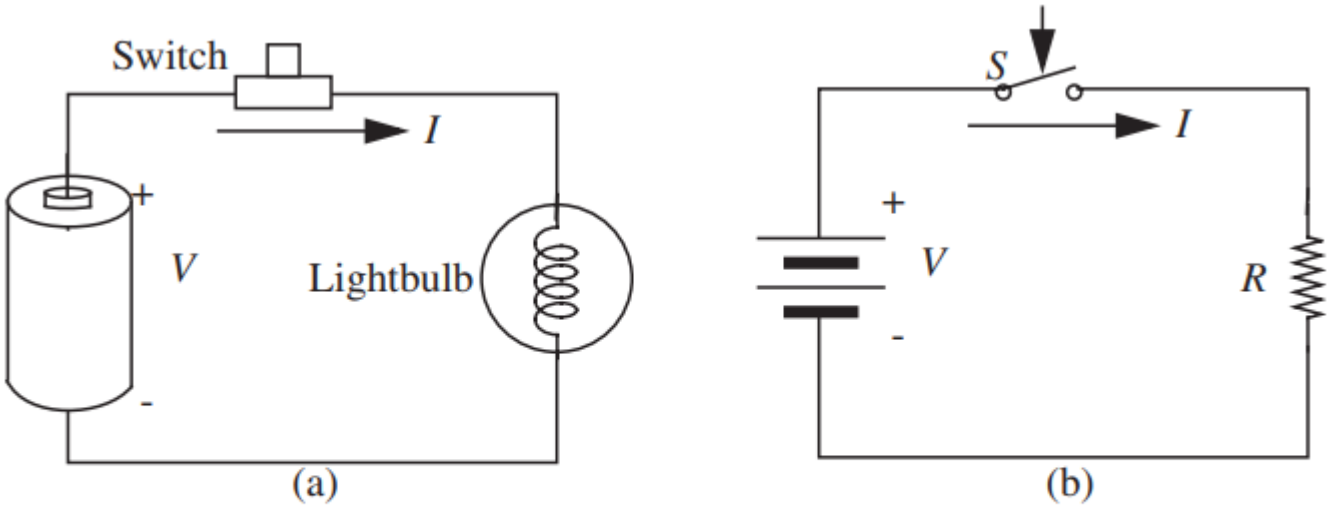
If we use combination of simple gates

A digital circuit



3 gates here

How to build a digital gate



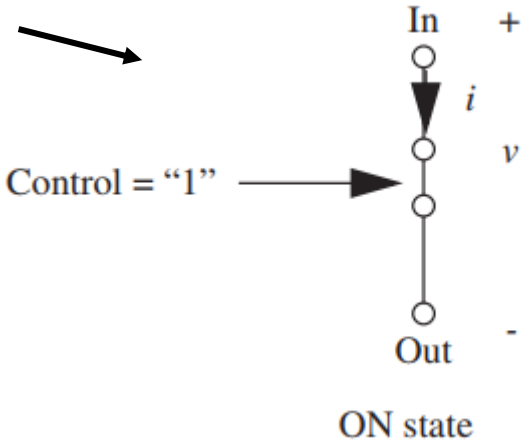
(a) The lightbulb circuit with a switch; (b) the lumped circuit representation.

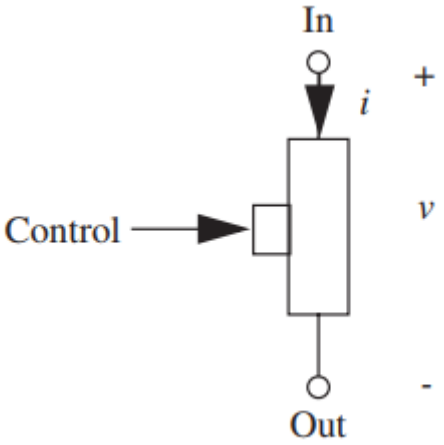
The switch is normally off and behaves like an open circuit. When pressure is applied to the switch, it closes and behaves like a wire and conducts current.

Accordingly, the switch can be modeled as the three-terminal device

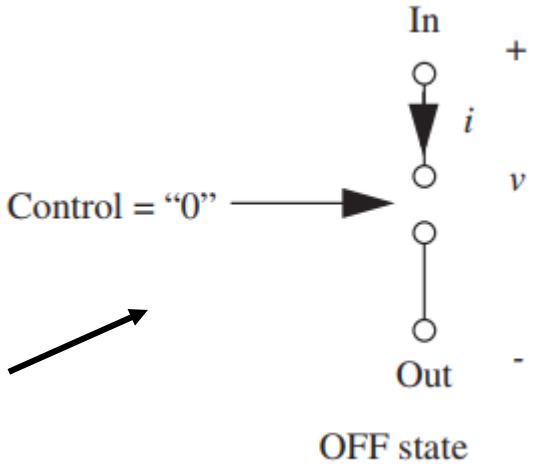
How to build a digital gate

When the control terminal has a TRUE or a logical 1 signal on it, the input is connected to the output through a short circuit.





Otherwise, there is an open circuit between the input and the output.



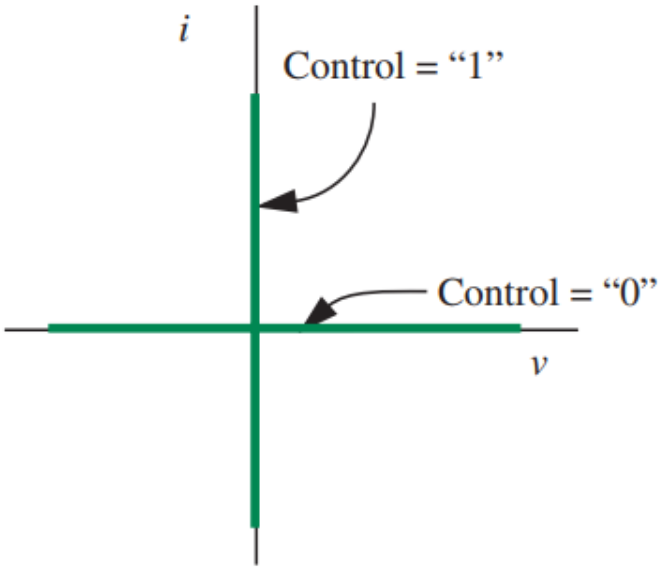
v-i Characteristis of the Switch

The *v*–*i* characteristics of a switch can also be expressed in algebraic form as:

$$\text{for Control} = \text{“0,”} \quad i = 0$$

and

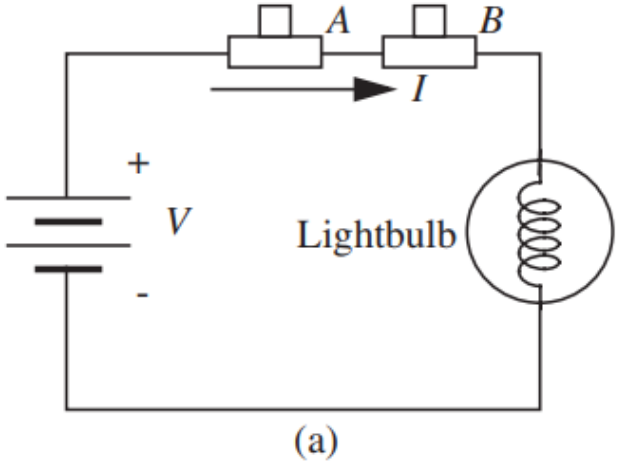
$$\text{for Control} = \text{“1,”} \quad v = 0.$$



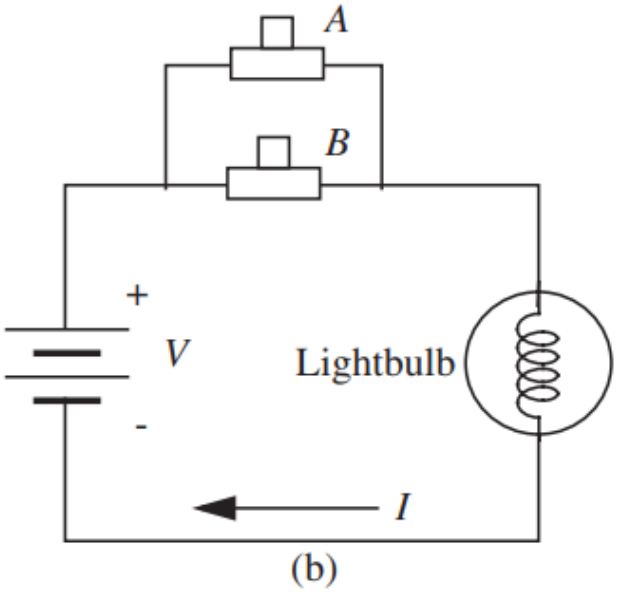
v–*i* characteristics of a switch. *v* is the voltage across the input and the output terminals of the switch and *i* is the current through the same pair of terminals.

Logic Functions using Switches

(a) The lightbulb circuit with switch in an *AND* configuration; (b) the lightbulb circuit with switches in an *OR* configuration.

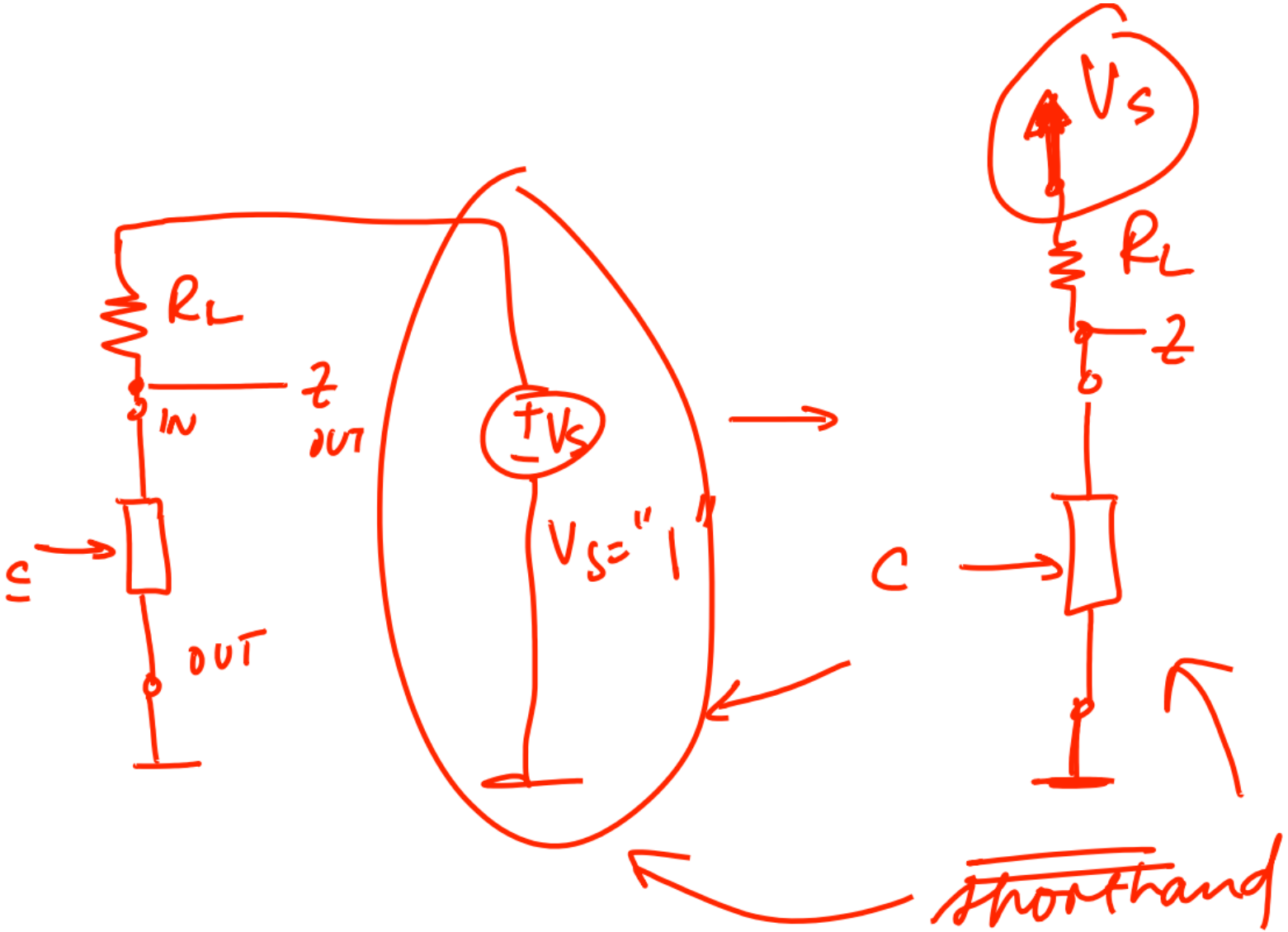


(a)

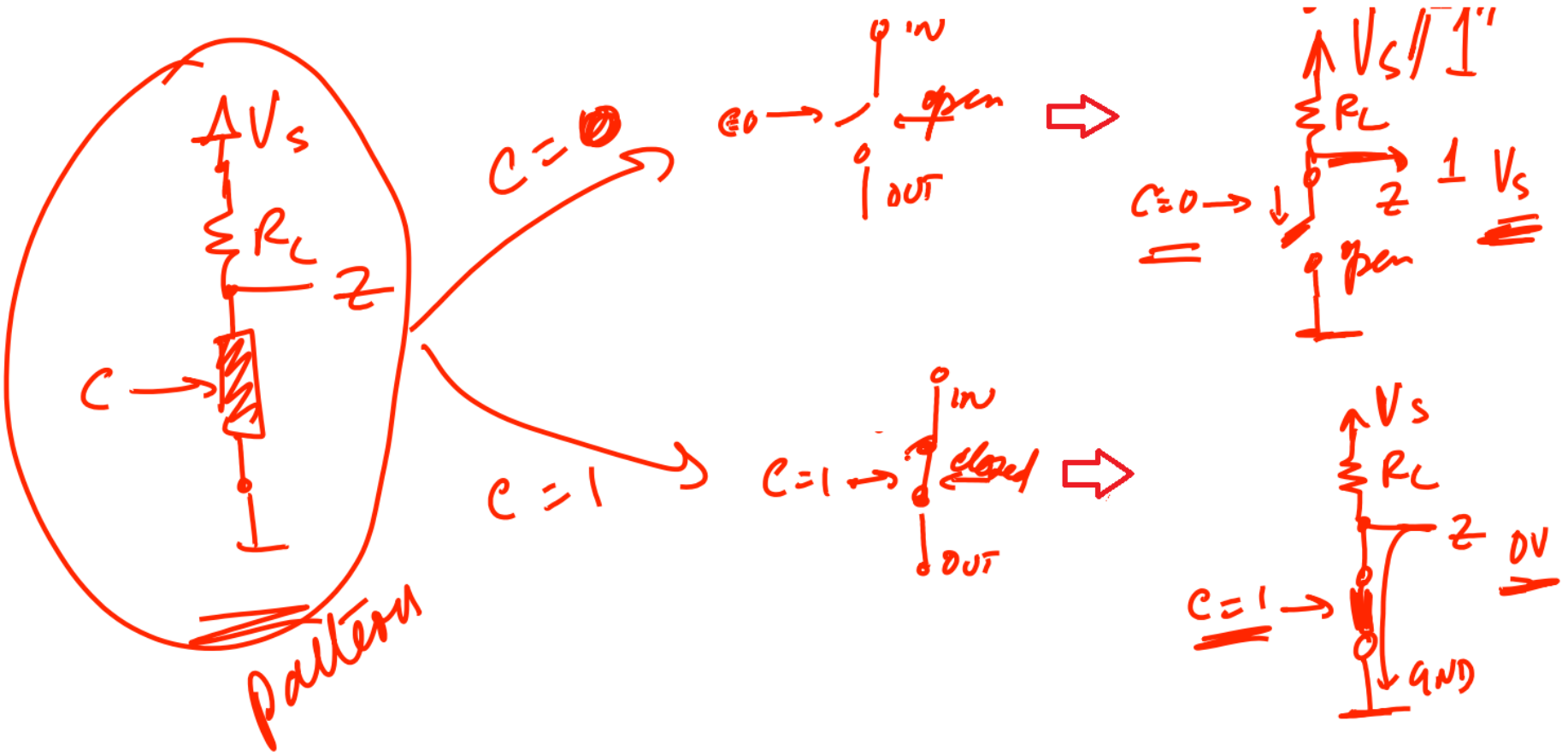


(b)

Using Three Terminal Switch Device



Behavior of this Basic Circuit

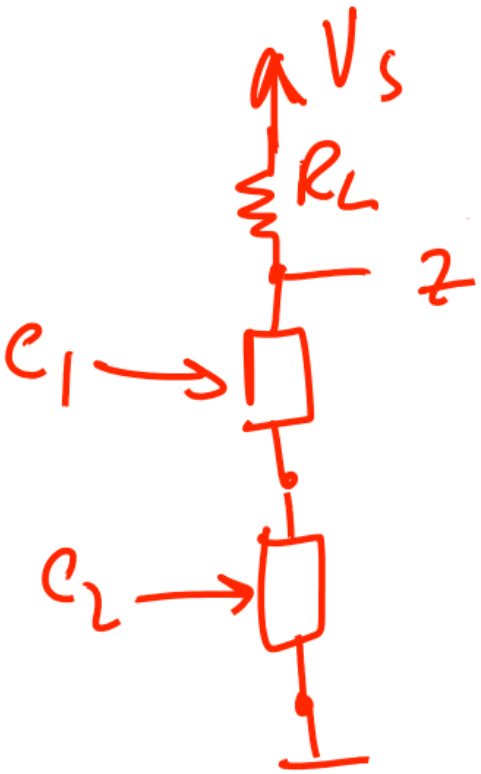


NOT Gate

eqvt.

C	Z
0	1
1	0

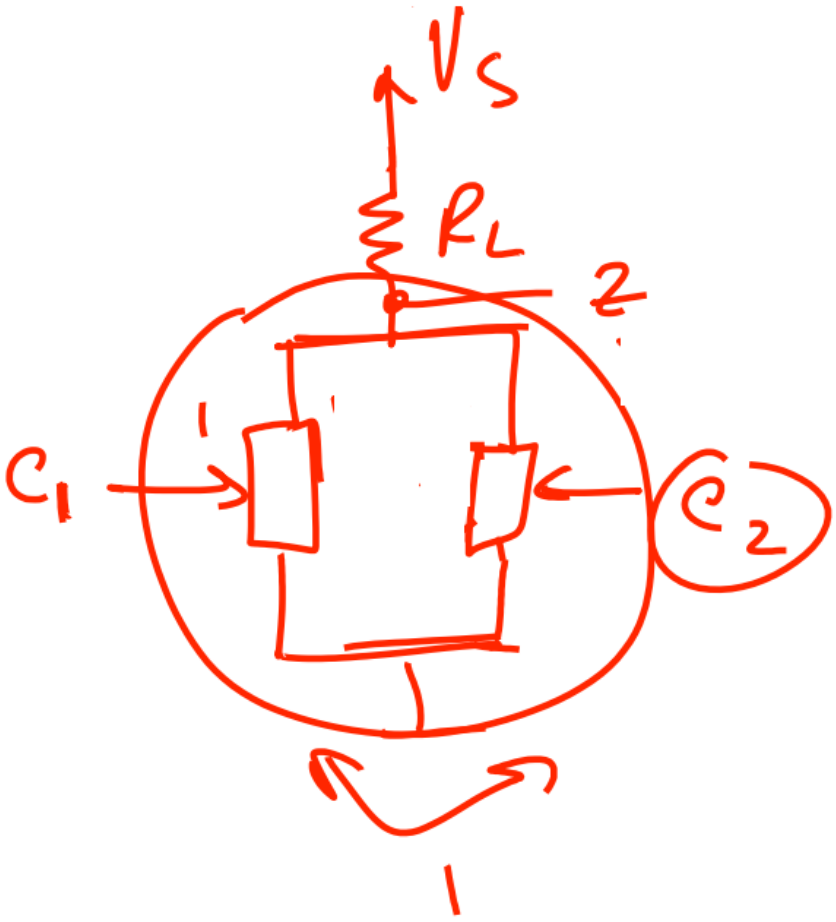
NAND Gate



C_1	C_2	Z
0	0	1
0	1	1
1	0	1
1	1	0

Truth table for

NOR Gate

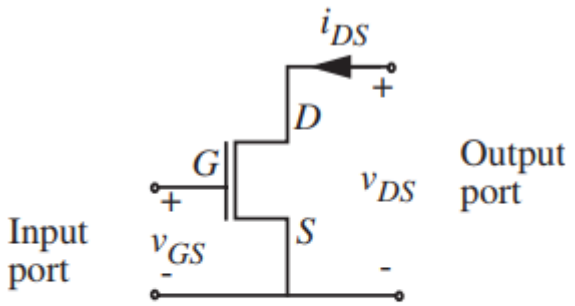


C_1 C_2	Z
0 0	1
0 1	0
1 0	0
1 1	0

Truth table for ?

The MOSFET Device

Metal-Oxide Semiconductor Field-Effect Transistor



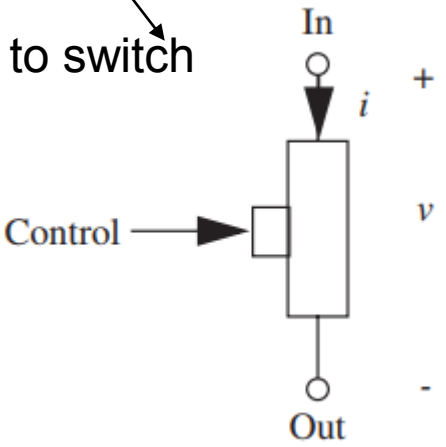
Port representation of a MOSFET.

3 terminal lumped element behaves like a switch

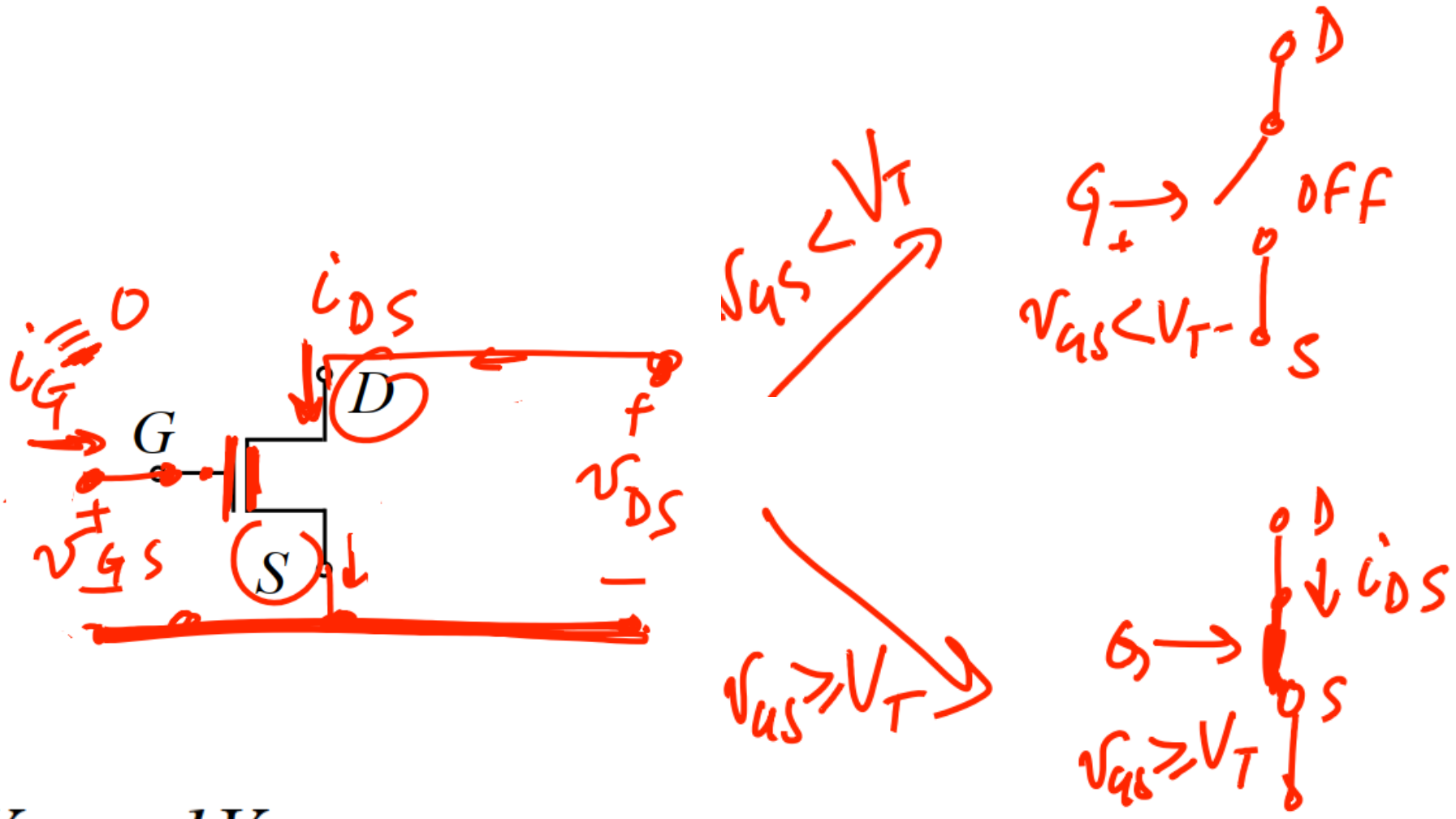
G: control terminal

D, S: behave in a symmetric manner (for our needs)

Similar to switch



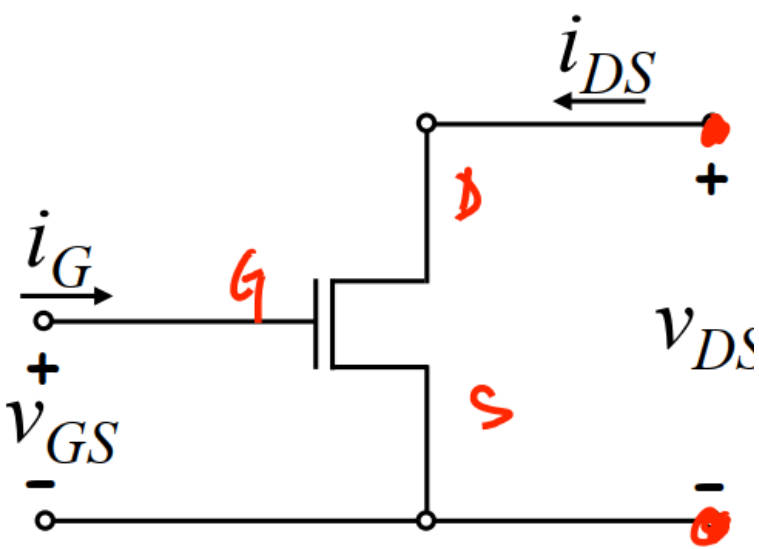
The MOSFET Device (S model)

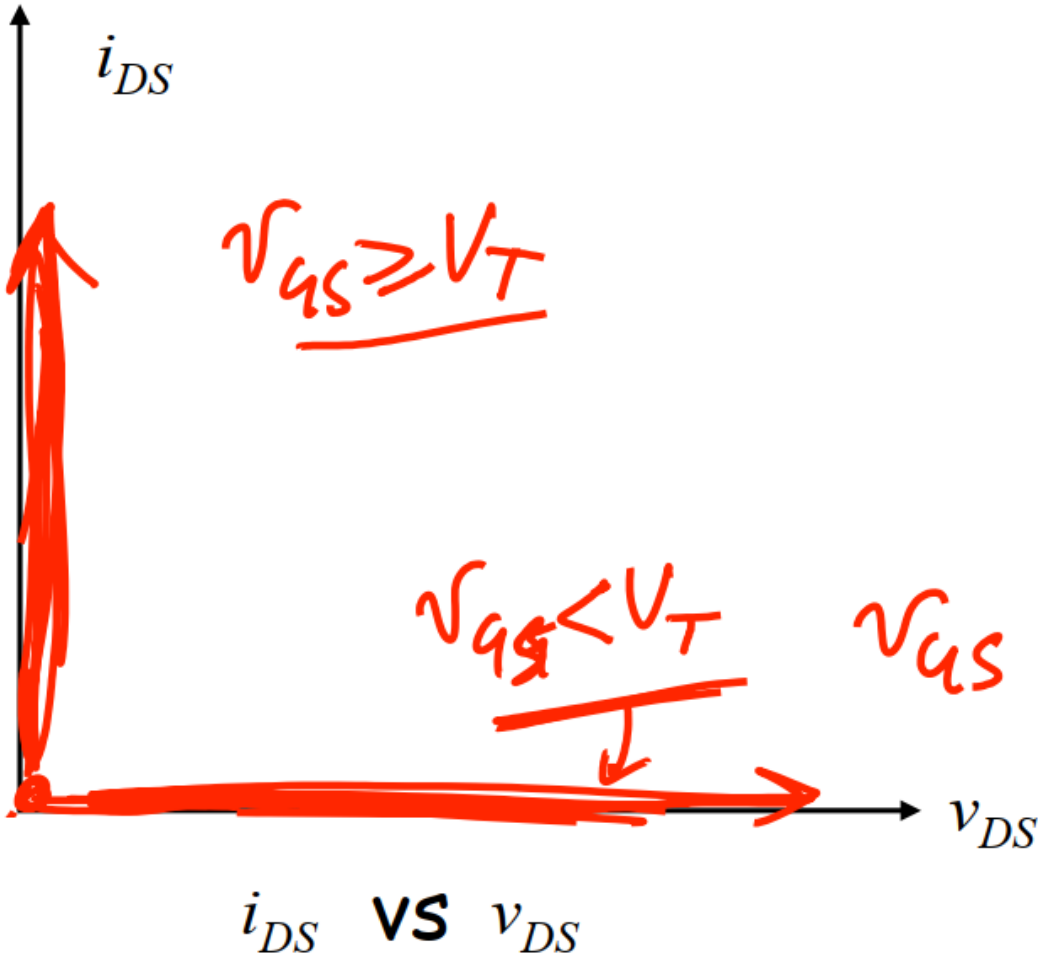


$V_T \sim 1V$

for example

MOSFET Device on Scope

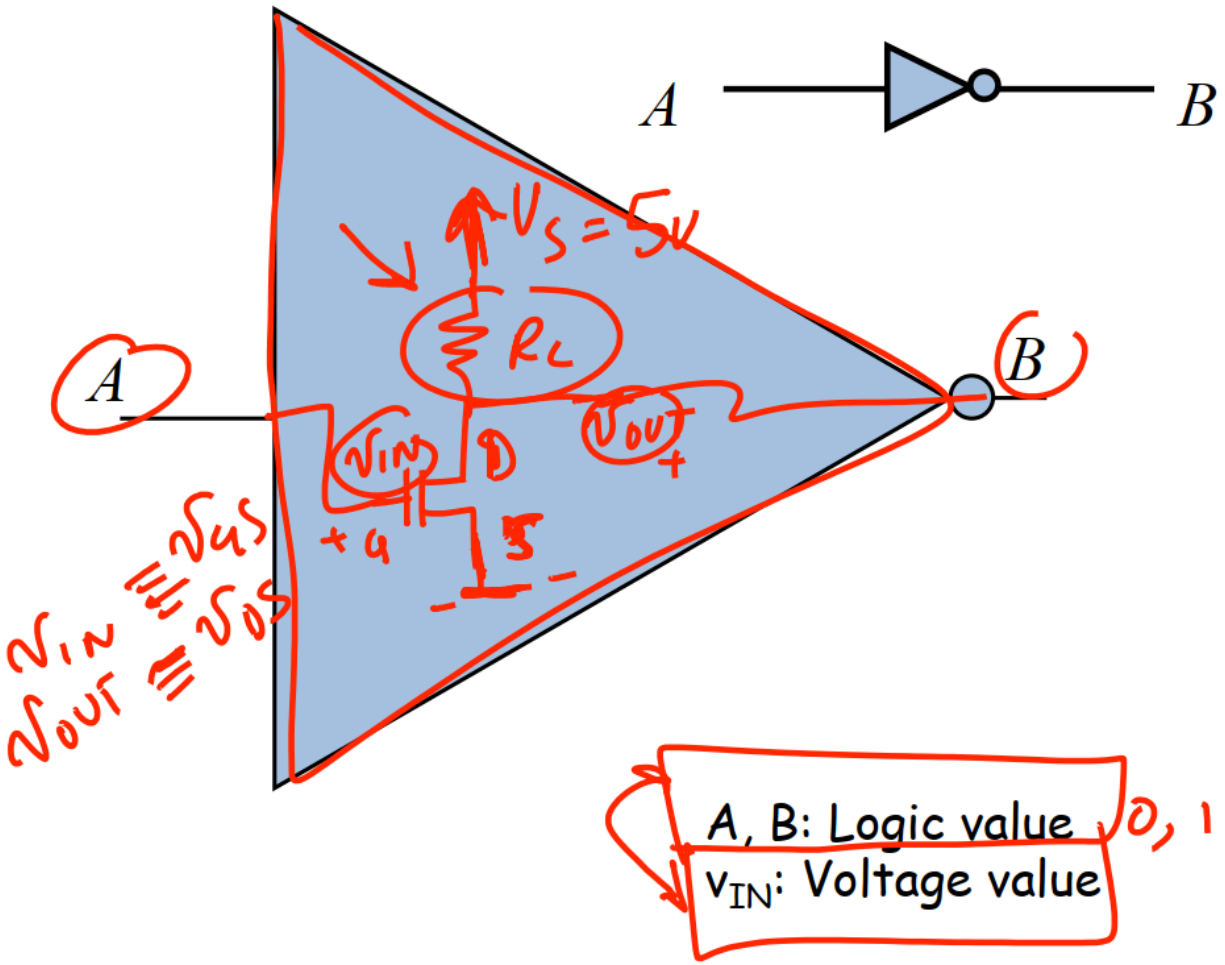




Consider two cases

i_{DS} **vs** v_{DS}

A MOSFET Inverter



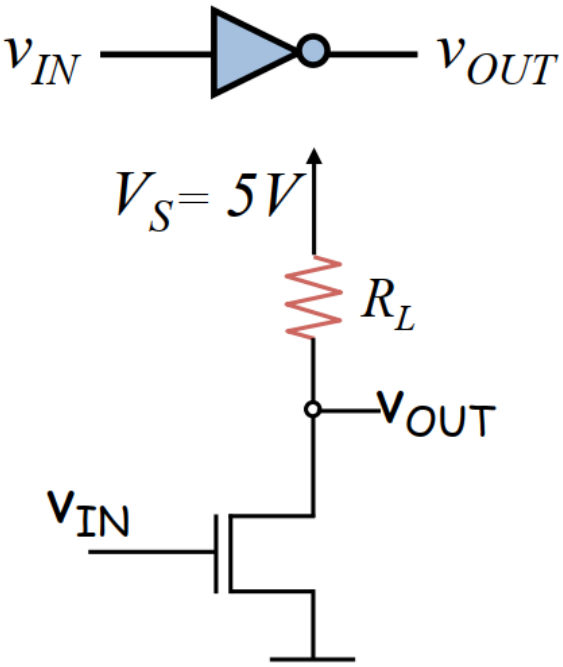
A, B: Logic value 0, 1

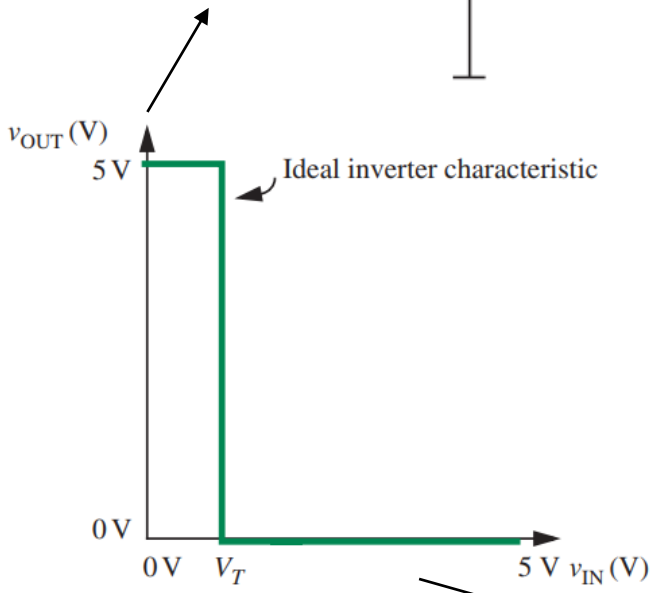
v_{IN}: Voltage value

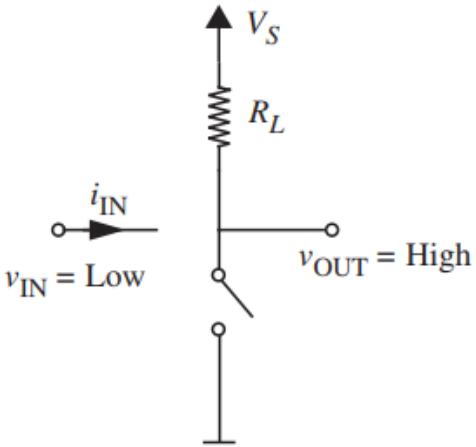
Note the power of abstraction:

The abstract inverter gate representation hides internal details such as power supply connections, R_L, GND, etc. When we build digital circuits, the ↑ and ⊥ are common across all gates!

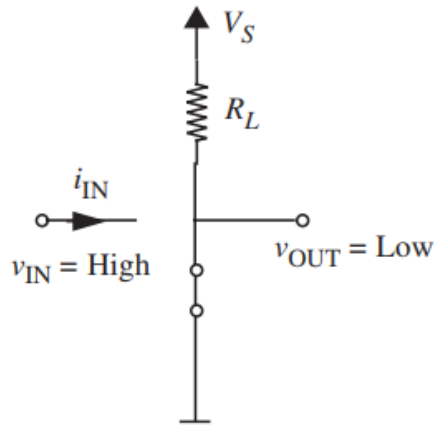
Input – Output Voltage Relation





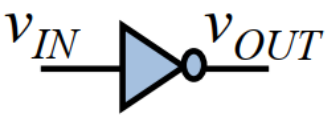


Called voltage transfer characteristic



An Inverter Design (Consider Static Discipline)

Question: The T1000 model laptop needs gates that satisfy a static discipline with voltage thresholds given below. Does our inverter qualify?

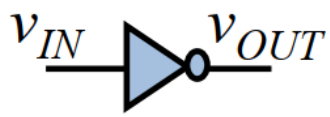


V_{OL} = 0.5V V_{IL} = 0.9V

V_{OH} = 4.5V V_{IH} = 4.1V

An Inverter Design (Consider Static Discipline)

Does our inverter satisfy the voltage thresholds for this static discipline?



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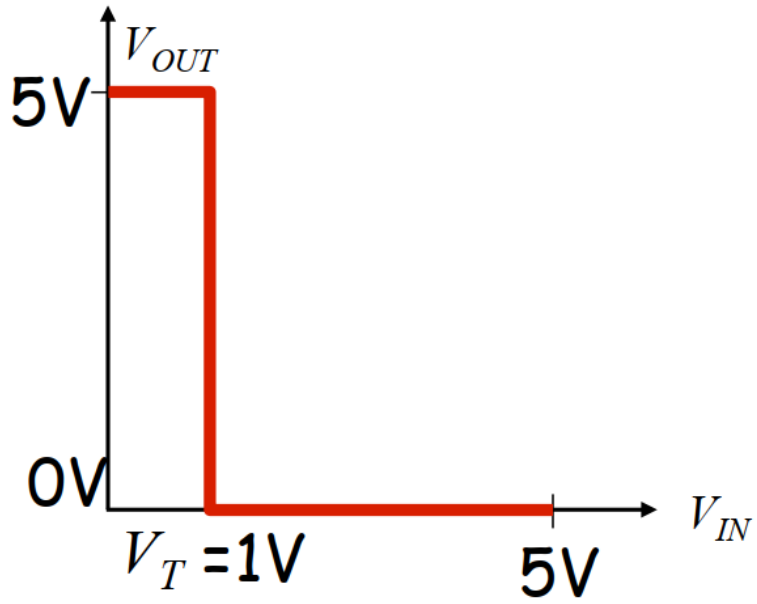
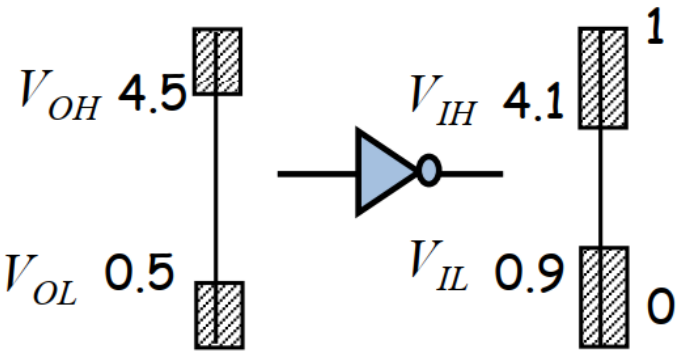
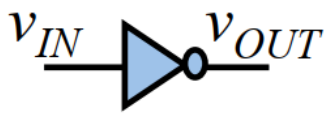
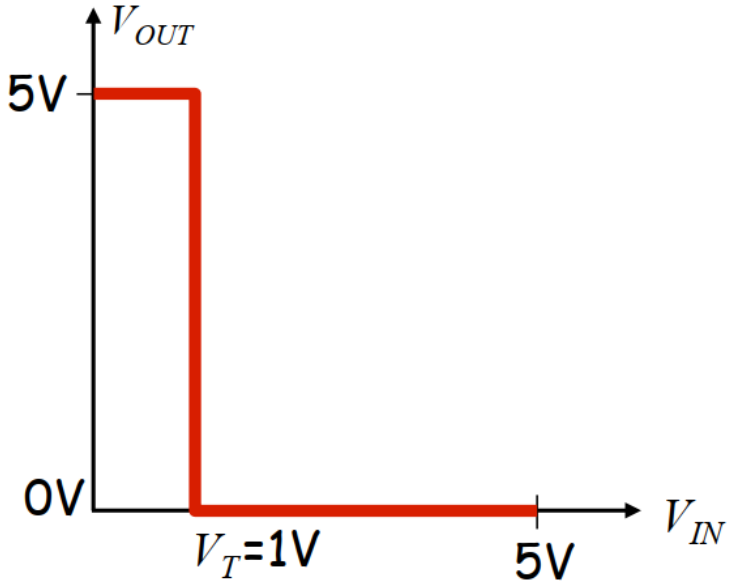




An Inverter Design (Consider Static Discipline)

Does our inverter satisfy the static discipline for these different thresholds?





V_{OL} = 0.2V V_{IL} = 0.5V

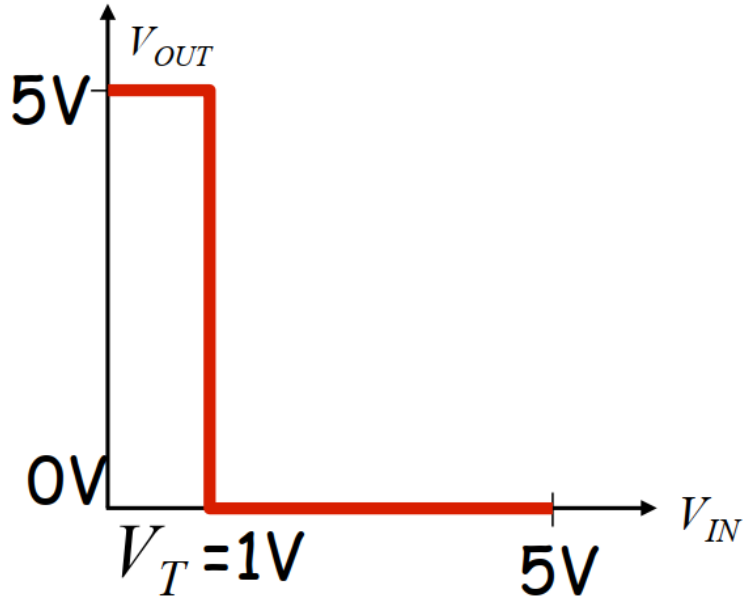
V_{OH} = 5.1V V_{IH} = 4.5V

V_{OL} = 0.2V V_{IL} = 0.5V

V_{OH} = 5.1V V_{IH} = 4.5V

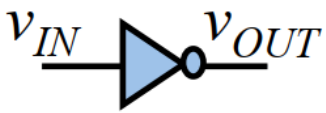
An Inverter Design (Consider Static Discipline)

How about these thresholds?



V_{OL} = 0.5V V_{IL} = 1.5V

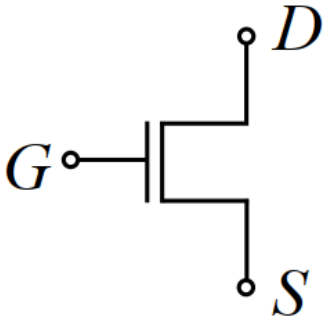
V_{OH} = 4.5V V_{IH} = 3.5V

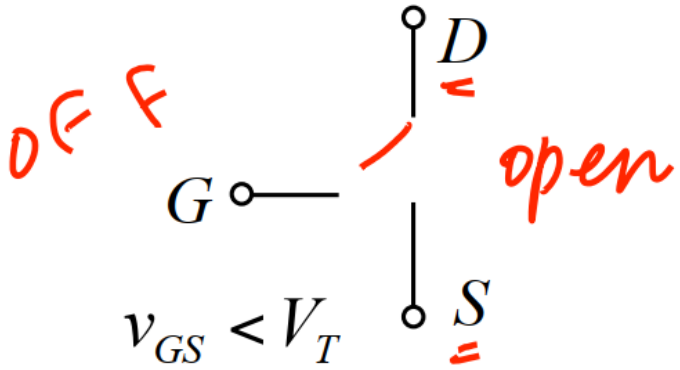


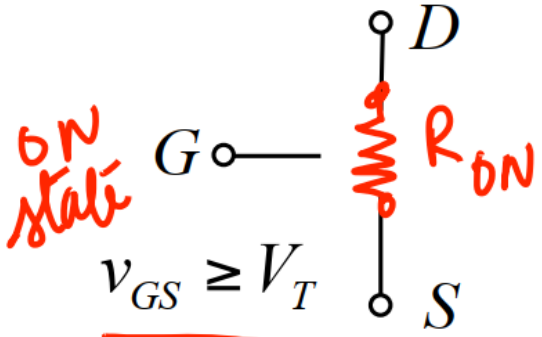
V_{OL} = 0.5V V_{IL} = 1.5V

V_{OH} = 4.5V V_{IH} = 3.5V

Switch-Resistor (SR) Model – More Accurate

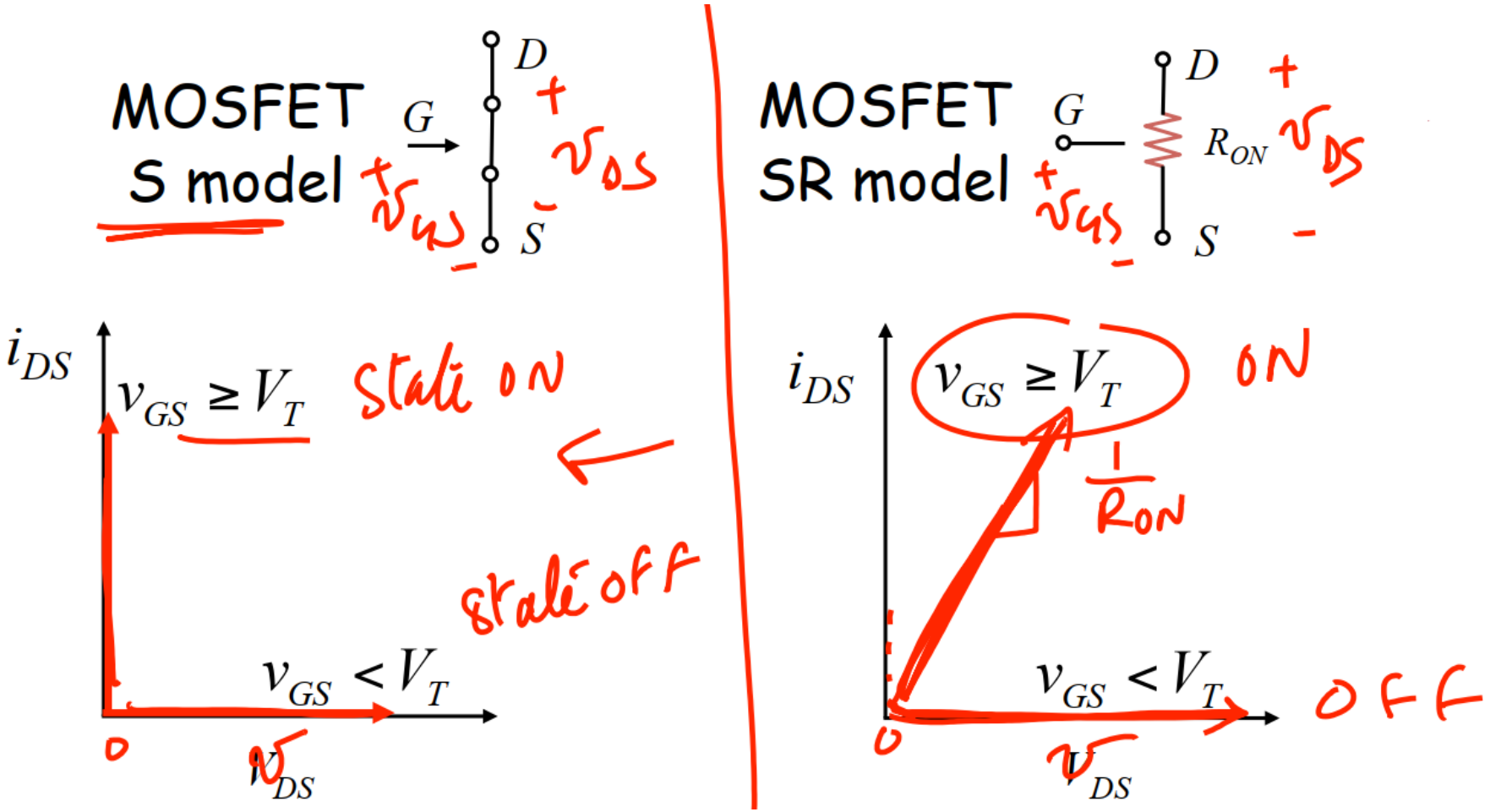




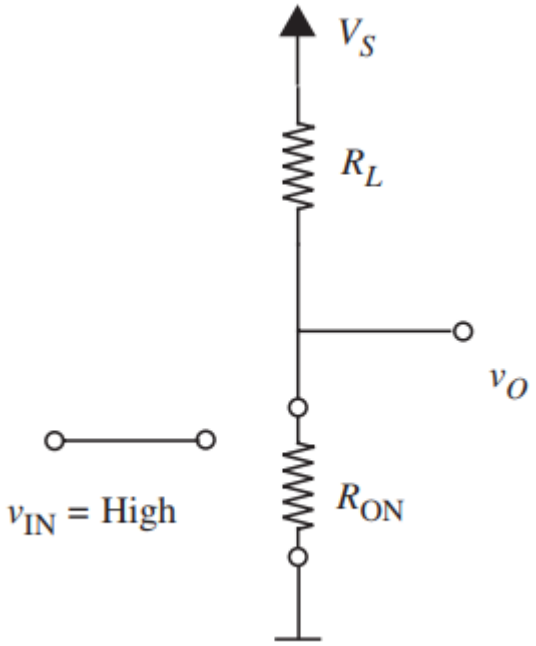


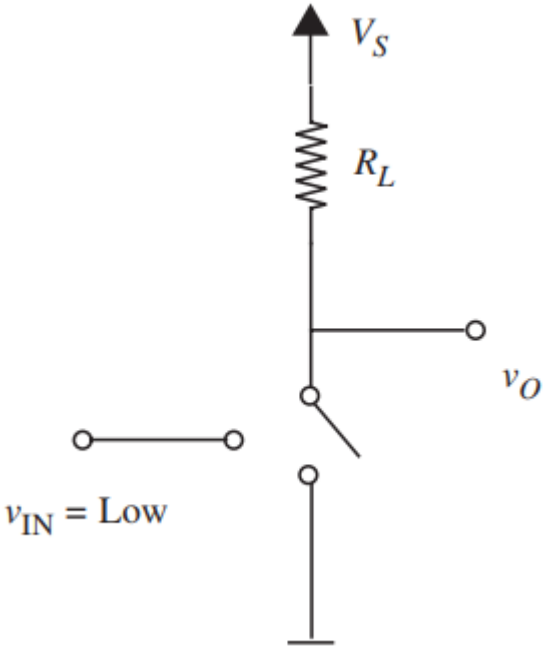
e.g. $R_{ON} = 5k\Omega$

SR Model of MOSFET



Using SR Model - Inverter





when the input v_{IN} is high (and above the threshold VT), the MOSFET is on and displays a resistance R_{ON} between its D and S terminals, thereby pulling the output voltage lower

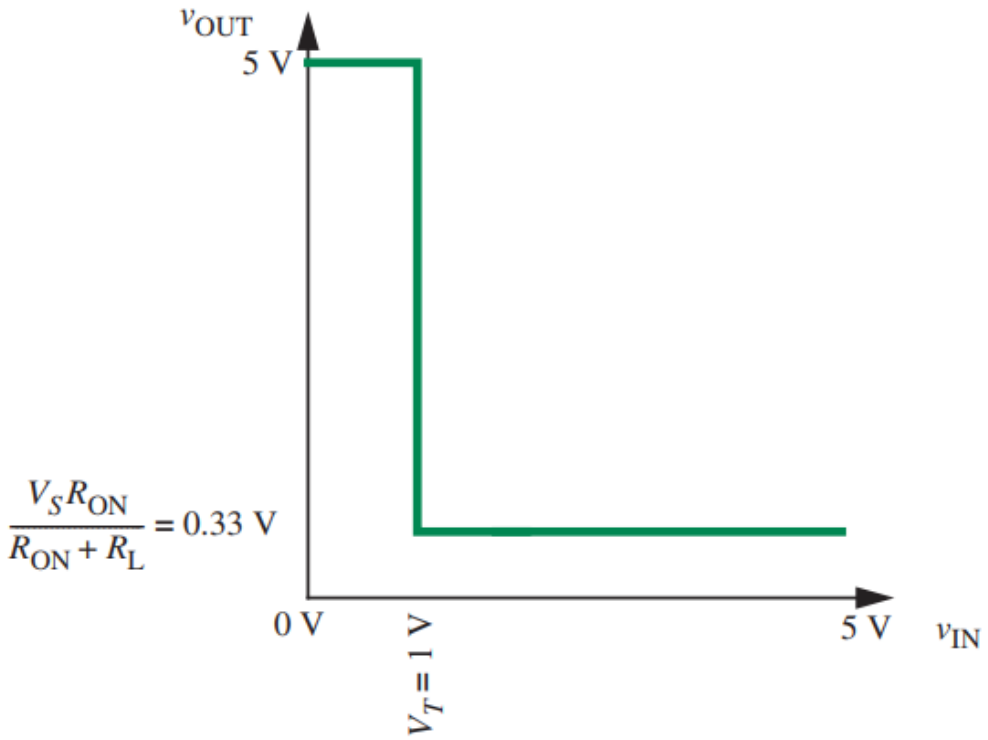
$$v_{OUT} = V_S \frac{R_{ON}}{R_{ON} + R_L}.$$

when the input is low, the MOSFET is off, and the output is raised to a high value

Using SR Model - Inverter

The resulting inverter transfer characteristics, assuming $V_S = 5$ V, $V_T = 1$ V, $R_{ON} = 1\,\text{k}\Omega$, and $R_L = 14\,\text{k}\Omega$, are shown in Figure. Notice that the lowest output voltage of the inverter is no longer 0 V, rather it is

$$V_S \frac{R_{ON}}{R_{ON} + R_L} = 0.33 \text{ V}.$$

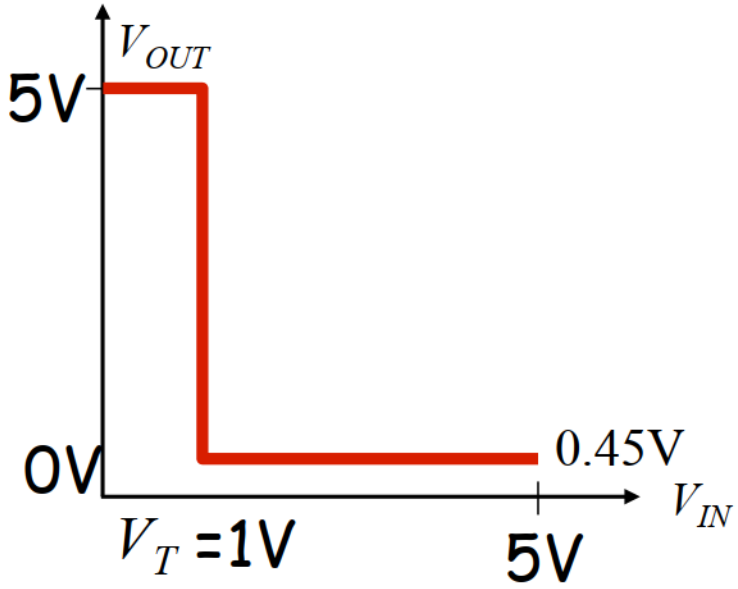


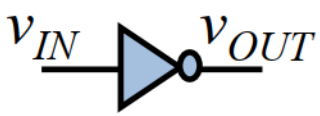
Inverter transfer characteristics using the SR model.

Static Discipline Criteria

When the R_L/R_{ON} ratio is 10.

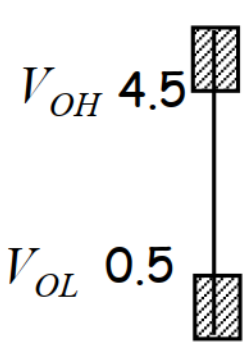
Does our inverter satisfy the voltage thresholds for this static discipline?

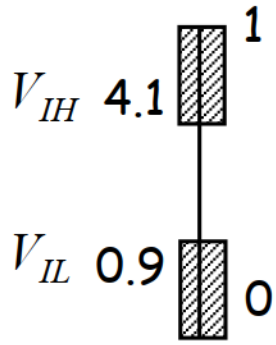




V_{OL} = 0.5V V_{IL} = 0.9V

V_{OH} = 4.5V V_{IH} = 4.1V

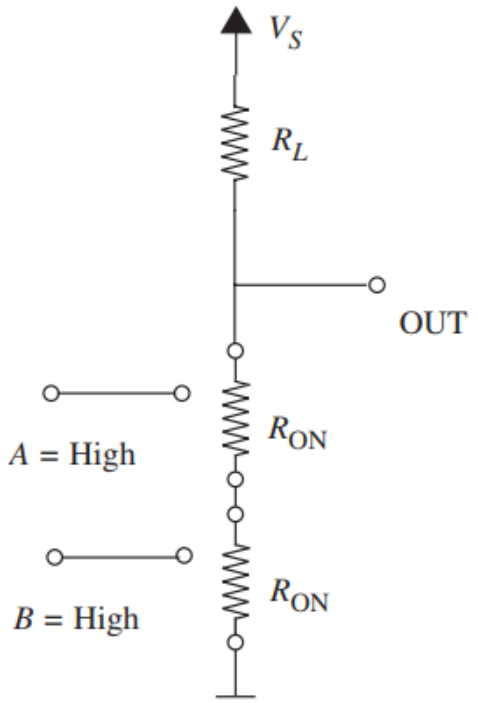




Static Power – NAND Gate Example

In this case, the output voltage when both inputs are high is given by

$$v_{OUT} = V_S \frac{2R_{ON}}{2R_{ON} + R_L}.$$



SR circuit model for NAND gate.